IKF6836 Data Sheet

Network Media Processor

Release 1.3

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Preliminary Information (Subject to Change)

47669 Fremont Boulevard
Fremont CA 94538
United States of America (USA)
1.510.979.0400 (Phone)
1.510.979.0500 (Facsimile)
http://www.ikanos.com/

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Document Status

The document status is shown on the bottom of each page. This describes the status of information in this document, which can be one of:

Advanced—Information on a product in early development.
Preliminary—Current information on a product under development.
Final—Complete information on a developed product.

Revision History

Version	Changes
Revision 0.5	Initial Draft
Revision 0.6	Revised Pin List, Functional Description Table, Pin Loading & Initial Configuration Tables
Revision 0.7	Revised Packaging Information
Revision 0.8	Revised Packaging Details; incorporated review from Marketing
Revision 0.9	Revised Hardware & Software Description
Revision 0.9a	Revised thermal performance information; added Power Up Latch table, diagram; updates to HW and SW architecture diagrams and descriptions
Revision 0.9b	Added resistance values, multiplexing details for alternate pin functions; redrawn timing diagrams; incorporated feedback from SW, VLSI teams
Revision 0.9c	Updated Pin description and modified timing diagrams.
Revision 1.0	Preliminary Data Sheet Released.
Revision 1.1	Dim A & Dim B values added in package outline
Revision 1.2.	Flash changed to 16MB max
Revision 1.3	USB supply pins swapped

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1 General Description

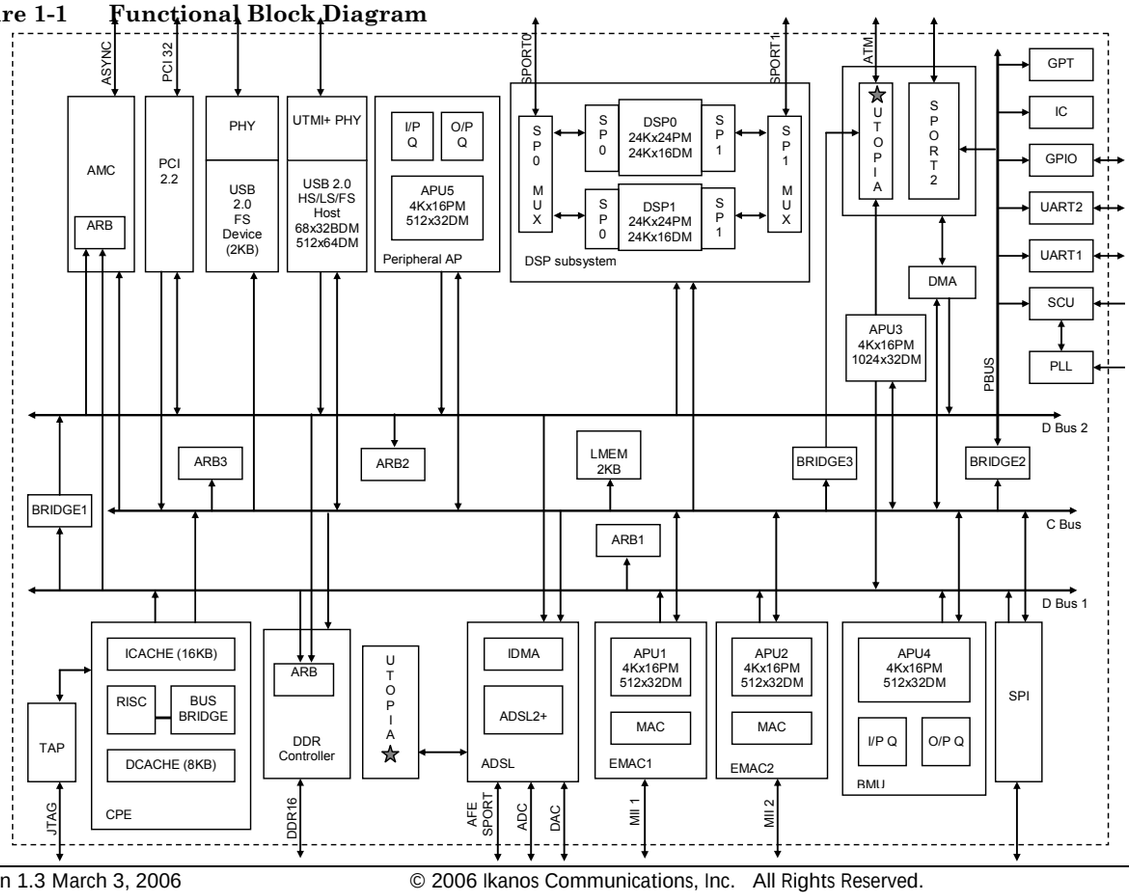
1.1 Overview

Fusiv® Vx160 (IKF6836) is a high-performance ADSL/ADSL2/ADSL2+ Network Media Processor for Voice and Data bundled services. It provides high-speed switching, routing, packet filtering and firewall functions.

The distinctive feature of Fusiv® Vx160, is the presence of micro-coded data path computing engines called Accelerator Processors, which provide hardware-like performance and software-like flexibility, giving it a capacity beyond that of conventional communications processors.

1.2 Functional Block Diagram

Figure 1-1 Functional Block Diagram



NOTES on the functional block diagram given in Figure 1-1:

1. APU stands for “Accelerator Processor Unit”
2. Data flows both ways between all units and buses
3. An arrow from unit to bus indicates whether the unit is a Master or Slave on the bus.
4. An arrow pointed towards the bus indicates the unit is a Master on the bus
5. An arrow pointed towards the unit indicates the unit is a Slave on the bus
6. UTOPIA block has an interface connection to the ADSL block as depicted by the ★
7. Buses:
   - Data Bus 1 – DBUS 1
   - Data Bus 2 – DBUS 2
   - Control Bus – CBUS
   - Peripheral Bus – PBUS
   - System Bus – SBUS
   - SBUS = DBUS 1 + DBUS 2 + CBUS
   - PM – Program Memory
   - DM – Data Memory
   - BDM – Buffer Descriptor Memory

1.3 Features

- Networking operations at ADSL2plus and Ethernet wire speeds
- Communication interfaces for Ethernet and ATM
- Provision to implement G.bond (ATM-based bonding)
- Integrated DSP and Micro controller with Embedded RAM for Programmability and Software Upgradeability
- Digital Timing Recovery using Sample-Rate Conversion eliminates the need for external VCXO
- Supports ATM and AAL5 with hardware SAR engine compliant with ATM Forum UNI 3.1/4.0, ITU-T I.356, I.361, I.362 and I.363

- Peripheral interfaces like SPI, PCI, UART and SPORT
- 200 MHz, 16-bit DDR interface
- 16-bit Asynchronous Memory Interface
- USB 2.0 full speed (FS) device with integrated PHY
- USB 2.0 HS/FS/LS Host (EHCI & OHCI) with integrated UTMI+ PHY
- Ability to handle 2 to 8 channels of voice, as well as data switching functions
- Flexibility to be deployed for a variety of VoIP applications
- Facilitates glue less interface to Blackfin processors
- IEEE 1149.1 compliant JTAG interface for debug
- 448 Lead Free - PBGA (Plastic Ball Grid Array) 23 x 23 package
- Operating Conditions – Commercial (0^0C to 70^0C)
- 3.3V and 2.5V I/O and 1.8V core power supply

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2 Specifications

2.1 Electrical Characteristics—DC

Table 2-1 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Digital I/O Supply	IVDD	3.0	3.3	3.6	V
Digital Core Supply	CVDD	1.75	1.8	1.85	V
DDR Digital I/O Supply	VDDQ	2.3	2.5	2.7	V
DDR Reference Voltage	VREF	1.15	1.25	1.35	V
Ambient Temperature	T_A	0	25	70	°C

Table 2-2 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage (IVDD)		-0.3		+ 3.6	V
Core Supply Voltage (CVDD)		-0.3		+ 2.0	V
Input Voltage		-0.5		IVDD + 0.5	V
Output Voltage Swing		-0.5		IVDD + 0.5	V
Ambient Temperature (Operating)		-40		+ 70	°C
Storage Temperature		- 65		+ 150	°C

Table 2-3 IKF6836 Thermal Characteristics

	Air Velocity (m/s)	Die Temp. (^{0}C)	θ_{JA} (^{0}C/W)	θ_{JC} (^{0}C/W)
No Thermal via in board	Still air	107.8	15.8	5.4
	1	102.4	13.5	
	2	100.8	12.8	
Thermal via in board	Still air	105.3	14.7	5.4
	1	99.7	12.4	
	2	98.1	11.7	

NOTE: * The measurements were made under test conditions of 70°C and 2.4W

Ambient Température Rating :

$T_J = T_{AM} + \theta_{JA} \times W_{MAX}$

T_{AM} = Ambient Temperature (i.e. com/ind/mil)

θ_{JA} = Thermal resistance from junction to ambience

θ_{JC} – Themal Resistance from junction to case

W_{MAX} = Maximum Wattage Dissipation from Die

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the IKF6836 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table 2-4 Jitter Specification

	ETH_PHY_CLK (25 MHz)	Processor Clock (100 MHz)	PCI Clock (33.33MHz)	ADSL2 clock (175/87.5MHz)	Unit
Period Jitter Peak-to-Peak	-TBD-	-TBD-	-TBD-	-TBD-	ps, rms
Period Jitter	-TBD-	-TBD-	-TBD-	-TBD-	ps, rms
Cycle-to-Cycle Jitter	-TBD-	-TBD-	-TBD-	-TBD-	ps, rms

Output Clock Jitter (cycle-to-cycle) at Fout=250MHz is typically 200 ps pk-pk

Output Clock Jitter (cycle-to-cycle) at Fout=500MHz is max.200 ps pk-pk

Table 2-5 Power Up Latch

Pad Name	Value at Power Up (in bold); Description	Parameter	Symbol	Min	Typ	Max	Unit
MII1_TX_DATA_0	**LOW**; HIGH – Boot via SPI. LOW – Boot via FLASH.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
MII1_TX_DATA_1	**LOW**; HIGH – PLL bypass. LOW – PLLs are enabled.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
MII1_TX_DATA_2	**LOW**; HIGH – ADSL Standalone mode LOW - Vox160 functional mode	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
MII1_TX_DATA_3	**LOW**; HIGH – UTMI PHY gets 12 MHz clock from GPIO[31] pad, if AFE_SYNCOUT power up value is HIGH. LOW – UTMI PHY gets 12 MHz clock from AN_XTAL_UTMI pad , if AFE_SYNCOUT power up value is HIGH.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
MII1_TX_EN	**LOW**; HIGH – 25 MHz clock coming from ETH_PHY_CLK pad input. LOW – 25 MHz clock coming from AN_XTAL_25 pad.	Setup Time	t_S	10			ns
		Hold Time	t_h	5			ns
MII2_TX_DATA_0	**LOW**; HIGH – UTMI scan chain is part of top level scan chain. LOW - UTMI scan chain is NOT part of top level scan chain.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
MII2_TX_DATA_1	**LOW**; HIGH – UTMI Production test mode enabled. LOW – UTMI Production test mode disabled.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
MII2_TX_DATA_2	**LOW**; HIGH – CPE jumps to FLASH address 0xbf000000 after reset. LOW – CPE jumps to FLASH address 0xbfC00000 after reset.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
MII2_TX_EN	**LOW**; HIGH – 35.328 MHz clock coming from AFE_MCLK pad input. LOW – 35.328 MHz clock coming from AN_XTAL_35 pad.	Setup Time	t_S	10			ns
		Hold Time	t_h	5			ns

AFE_SEN	**LOW**; HIGH – ADSL JTAG is selected. LOW - ADSL JTAG is NOT selected.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
AFE_SYNCOUT	**LOW**; HIGH – UTMI gets 12 MHz clock. LOW – UTMI gets 40 MHz clock.	Setup Time	t_S	10			ns
		Hold Time	t_h	5			ns
AFE_DAC_0	**LOW**; HIGH – Processor PLL is Power Down. LOW – Processor PLL is Active.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
AFE_DAC_1	**LOW**; HIGH – USB PLL is Power Down. LOW – USB PLL is Active.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
AFE_DAC_2	**LOW**; HIGH – ADSL PLL is Power Down LOW – ADSL PLL is Active.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
AFE_DAC_3	**LOW**; HIGH – DSP PLL is Power Down. LOW – DSP PLL is Active.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
AFE_DAC_4	**LOW**; HIGH – PCI PLL is Power Down. LOW – PCI PLL is Active.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
AFE_DAC_5	**HIGH**; HIGH – DSP PLL input coming from SPHY_XTAL pad (35.328 MHz). LOW – DSP PLL input coming from GPIO[30] pad.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
AFE_DAC_6	**LOW**; HIGH – PLL Debug mode enabled. LOW – PLL Debug mode disabled.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns
AFE_DAC_7	**LOW**; HIGH – ATM Pair Bonding enabled. LOW – ATM Pair Bonding disabled.	Setup Time	t_S	10			ns
		Hold Time	t_h	1			ns

Figure 2-1 Power Up Latch

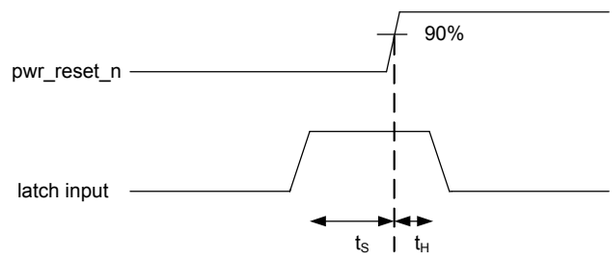


Table 2-6 PinLoading

Interface	Parameter	Symbol	Min	Typ	Max	Unit
JTAG	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			25	pF
USB	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			20	pF
MII	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			8	pF
MDI	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			15	pF
DDR	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			15	pF
AMC Address & Control	External Pin Loading	C_{Load}			25	pF
AMC Data	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			20	pF
UTOPIA	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			11	pF
PCI AD [31:0]	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			20	pF
PCI point-to-point	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			15	pF
PCI (other pads)	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			20	pF
SPORT	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			10	pF
SPORT2	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			10	pF
SPI	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			25	pF
GPIO	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			20	pF
AFE_DAC	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			15	pF
AFE_ADC	Input Pin Capacitance	C_{IN}	3		5	pF
	External Pin Loading	C_{Load}			15	pF

Table 2-7 Recommended Operating Conditions (IOL/IOH values)

Pin	Parameter	Symbol	Driver	Min	Typ	Max	Unit
GPIO [0-23]	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
GPIO [24-28]	Low level output current @ V_{OL} =0.4V	I_{OL}	16 mA	26.56	45.31	59.45	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	16 mA	-15.73	-32.50	-42.42	mA
GPIO [29-31]	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
JTAG_*	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
UART_*	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
MII_*	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
MDI_*	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
ETH_PHY_CLK	Low level output current @ V_{OL} =0.4V	I_{OL}	16 mA	26.56	45.31	59.45	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	16 mA	-15.73	-32.50	-42.42	mA
UTP_CLK	Low level output current @ V_{OL} =0.4V	I_{OL}	16 mA	26.56	45.31	59.45	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	16 mA	-15.73	-32.50	-42.42	mA
UTP (other pads)	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
SPI_*	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
SPORT_*	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
AMC_*	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA
AFE_*	Low level output current @ V_{OL} =0.4V	I_{OL}	8 mA	15.93	27.19	35.67	mA
	High level output current @ V_{OH} =2.4V	I_{OH}	8 mA	-9.441	-19.50	-25.45	mA

2.2 Electrical Characteristics—AC

2.2.1 MII Carrier Sense Interface

Table 2-8 MII (100 Mbps Carrier Sense Assertion / De-assertion Parameter)

Symbol	Parameter	Min	Typ	Max	Unit
t_1	MII_TX_EN sample asserted to MII_CAR_SNS assert	0		160	ns
t_2	MII_TX_EN deasserted to MII_CAR_SNS deassert	0		160	ns

Figure 2-2 MII (100 Mbps) Carrier Sense Assertion/De-Assertion

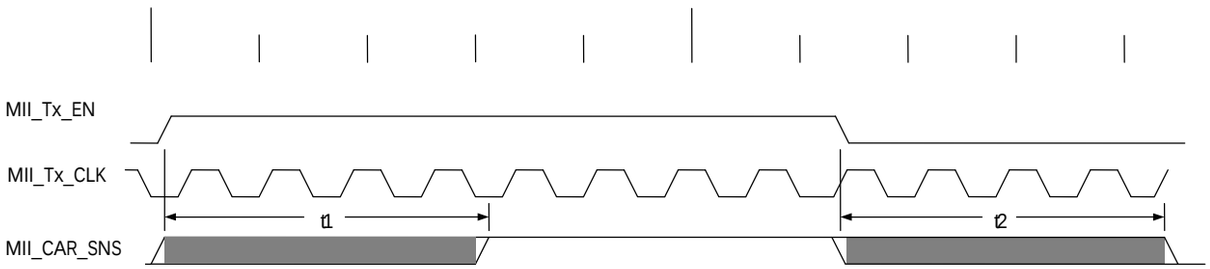


Table 2-9 MII (100 Mbps) Synchronous Receive Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_1	MII_RX_DATA[3:0] setup to MII_RX_CLK	10			ns
t_2	MII_RX_DATA[3:0] hold from MII_RX_CLK	10			ns
t_3	MII_RX_EN setup to MII_RX_CLK	10			ns
t_4	MII_RX_EN hold from MII_RX_CLK	10			ns
t_5	MII_RX_ERR setup to MII_RX_CLK	10			ns
t_6	MII_RX_ERR hold from MII_RX_CLK	10			ns

Figure 2-3 MII (100 Mbps) Synchronous Receive

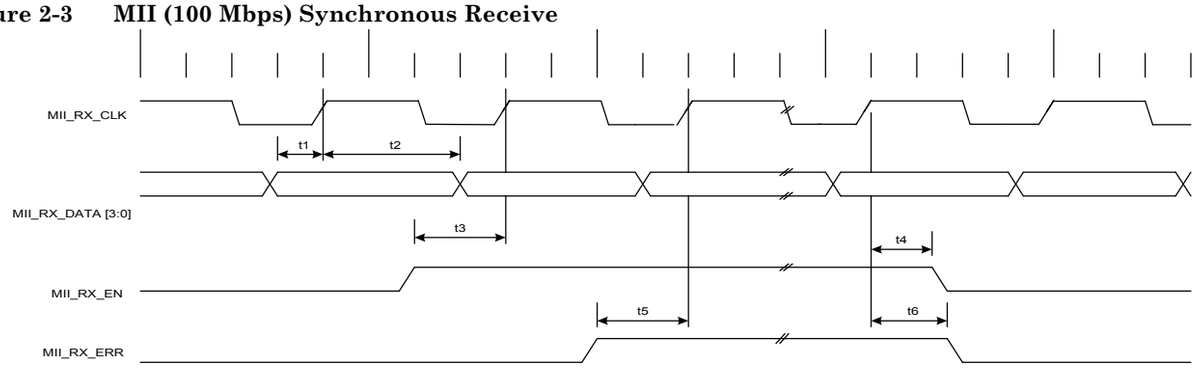


Table 2-10 MII (100 Mbps) Synchronous Transmit Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_1	MII_TX_CLK to MII_TX_DATA[3:0] delay	0		15	ns
t_2	MII_TX_CLK to MII_TX_EN delay	0		15	ns
t_3	MII_TX_CLK to MII_TX_ERR delay	0		15	ns

Figure 2-4 MII (100 Mbps) Synchronous Transmit

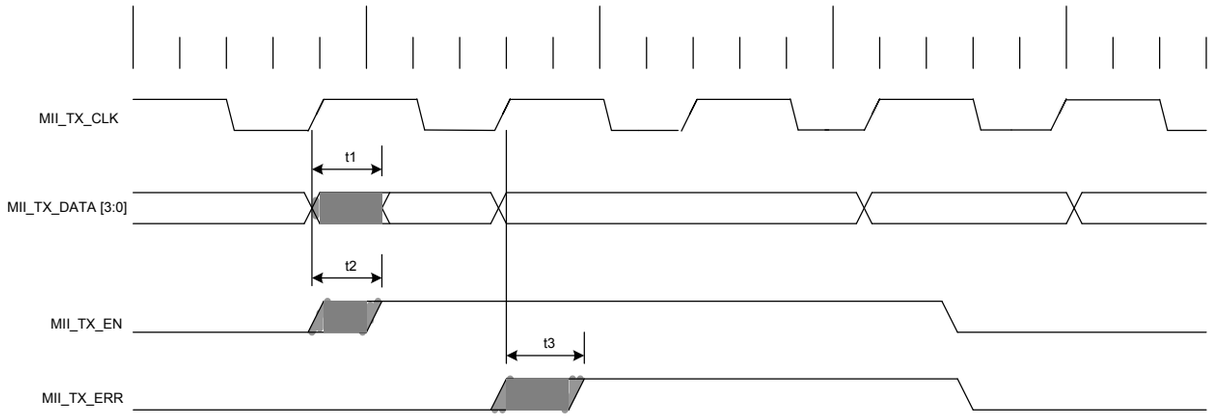


Table 2-11 MII (10 Mbps) Carrier Sense Assertion / Deassertion Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_1	MII_TX_EN asserted to MII_CAR_SNS assert	0		800	ns
t_2	MII_TX_EN deasserted to MII_CAR_SNS deassert	0	800	1600	ns

Figure 2-5 MII (10 Mbps) Carrier Sense Assertion / De-assertion

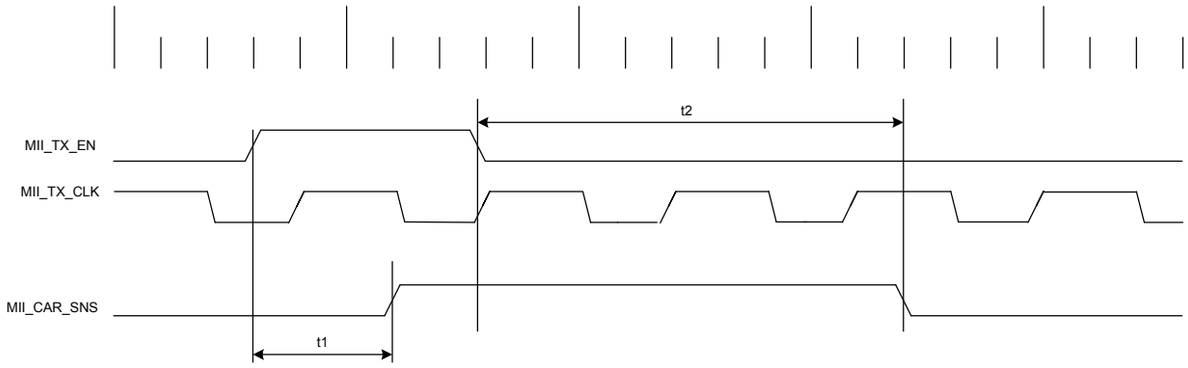


Table 2-12 MII (10 Mbps) Synchrnous Transmit Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_1	MII_TX_DATA[3:0], MII_TX_EN, MII_TX_ERR setup to MII_TX_CLK rise	375			ns
t_2	MII_TX_DATA[3:0], MII_TX_EN, MII_TX_ERR hold after MII_TX_CLK rise	0			ns

Figure 2-6 MII (10 Mbps) Synchronous Transmit

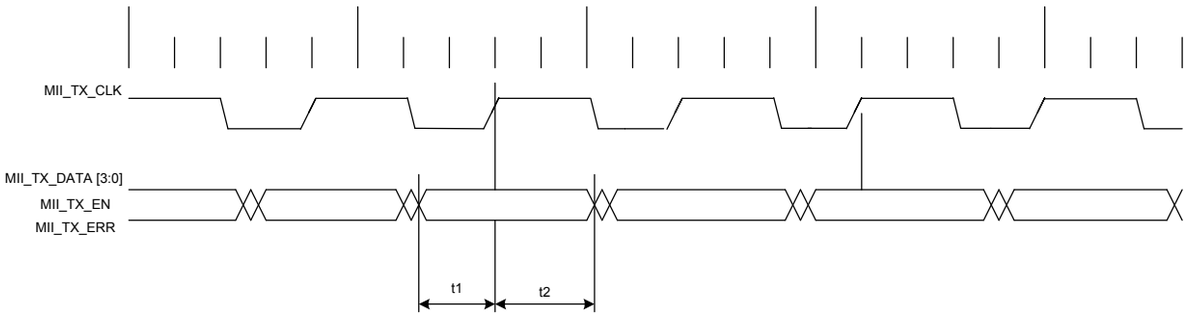
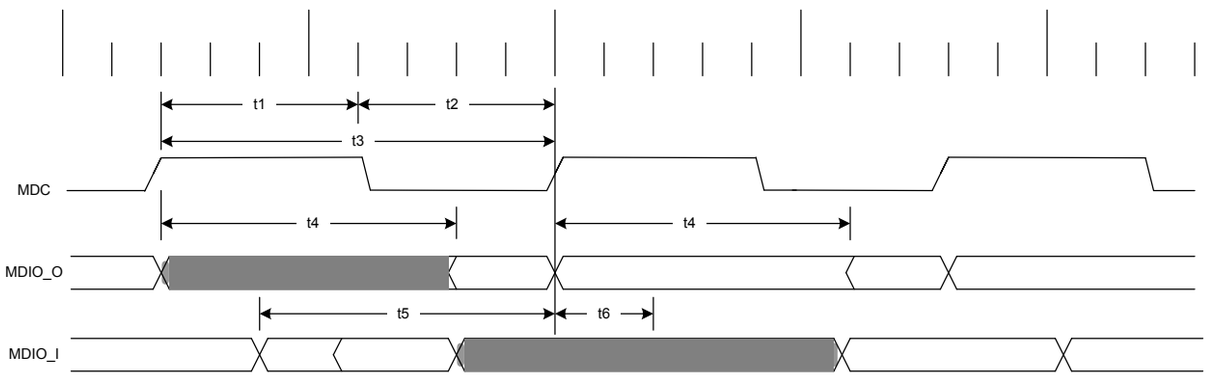


Table 2-13 MII Management Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_1	MDC minimum high time	160			ns
t_2	MDC minimum low time	160			ns
t_3	MDC period	400			ns
t_4	MDC rise time to MDIO valid	0		300	ns
t_5	MDIO setup time to MDC	10			ns
t_6	MDIO hold time from MDC	10			ns

Figure 2-7 MII Management

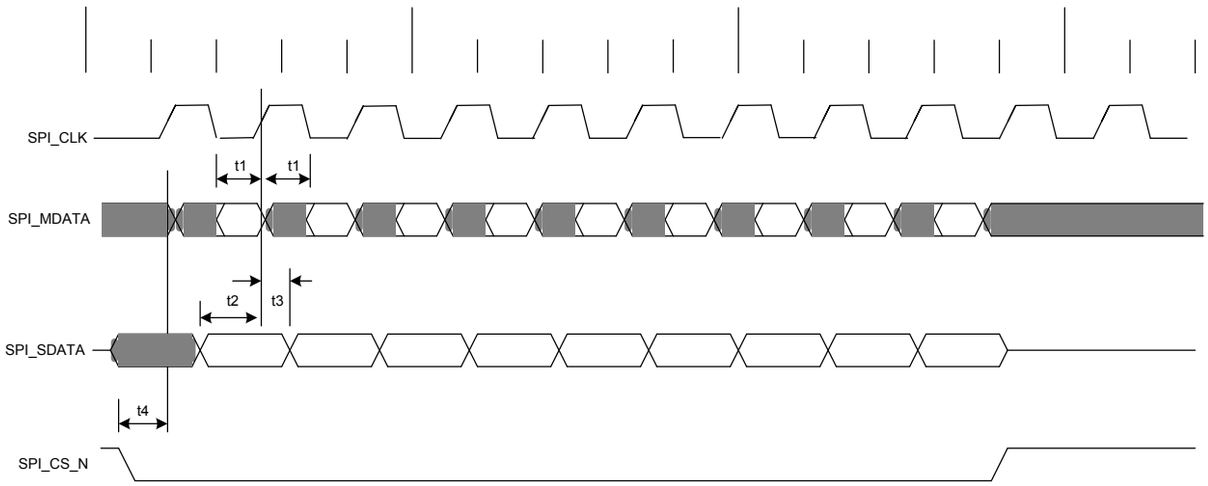


2.2.2 SPI Interface

Table 2-14 SPI Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_1	SPI_CLK to SPI_MDATA delay	3		16	ns
t_2	SPI_SDATA setup time	20			ns
t_3	SPI_SDATA hold time	1			ns
t_4	SPI_CS_N setup time	16			ns

Figure 2-8 SPI

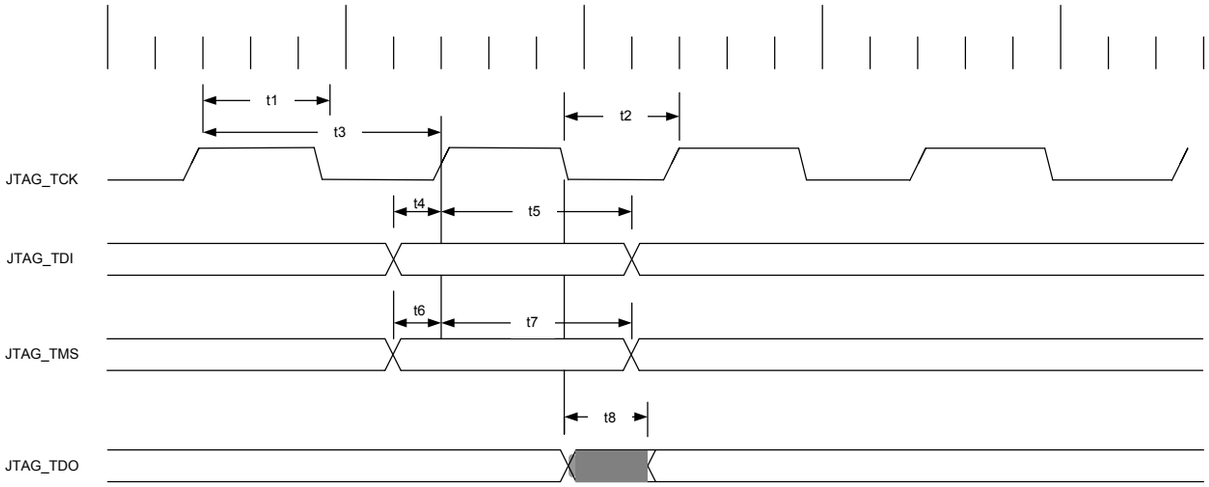


2.2.3 JTAG Interface

Table 2-15 JTAG Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_1	JTAG_TCK rise time	12.5			ns
t_2	JTAG_TCK fall time	12.5			ns
t_3	JTAG_TCK period	25			ns
t_4	JTAG_TDI setup time to JTAG_TCK	5			ns
t_5	JTAG_TDI hold time from JTAG_TCK	5			ns
t_6	JTAG_TMS setup time to JTAG_TCK	5			ns
t_7	JTAG_TMS hold time from JTAG_TCK	5			ns
t_8	JTAG_TCK NEGEDGE to JTAG_TDO delay	0			ns

Figure 2-9 JTAG



2.2.4 UTOPIA Interface

Table 2-16 UTOPIA Transmit Parameter (at UTP_CLK 25 MHz)

Symbol	Parameter	Min	Typ	Max	Unit
t_1	UTP_CLK to UTP_TX_SOC delay	1			ns
t_2	UTP_CLK to UTP_TX_EN delay	1			ns
t_3	UTP_CLK to UTP_TX_DATA delay	1			ns
t_4	UTP_TX_CLAV setup time to UTP_CLK	10			ns
t_5	UTP_TX_CLAV hold time from UTP_CLK	1			ns

Figure 2-10 UTOPIA Transmit

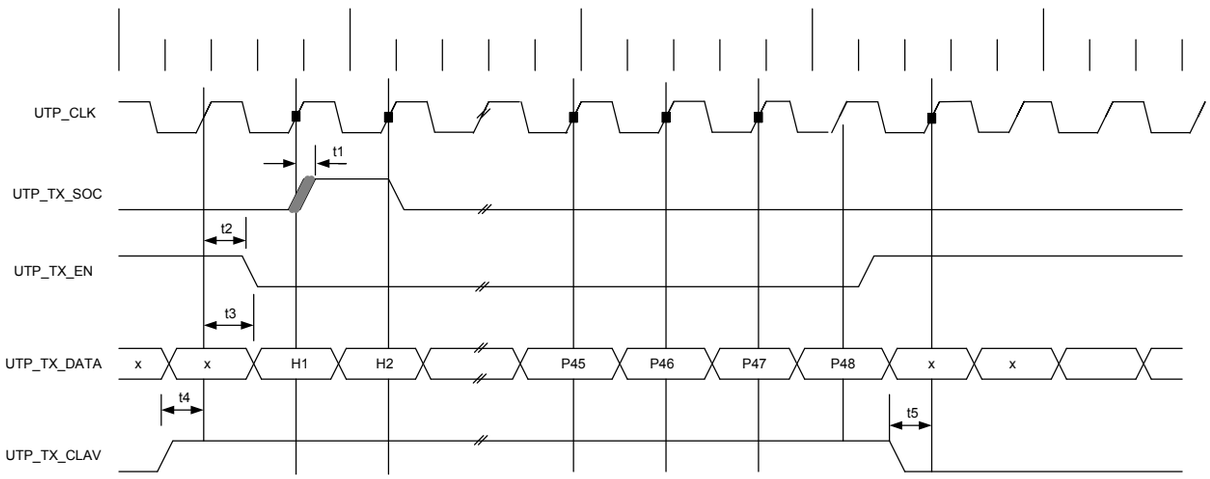
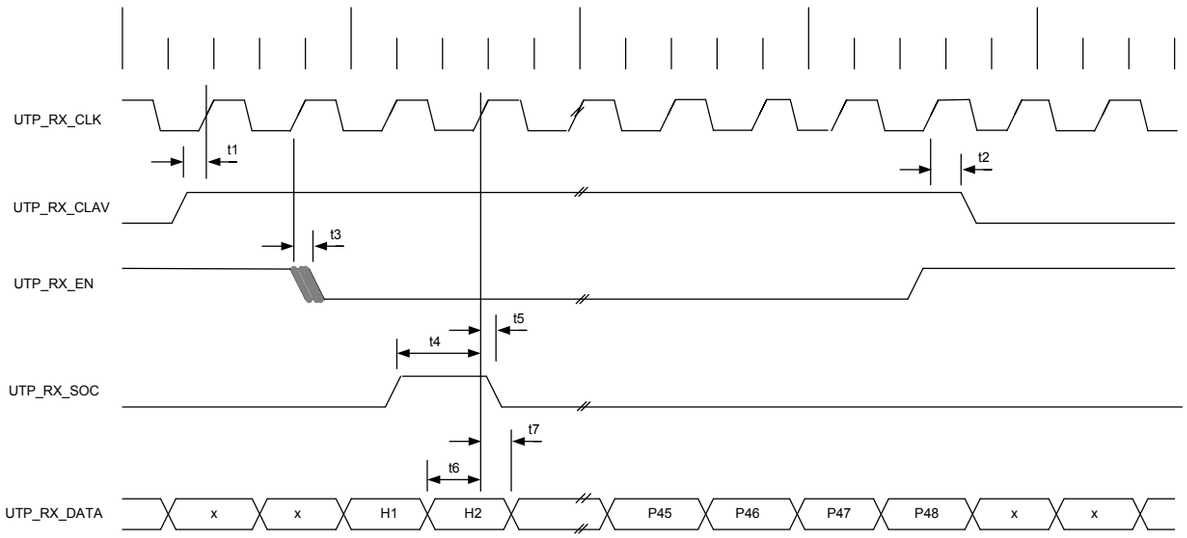


Table 2-17 UTOPIA Receive Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_1	UTP_RX_CLAV setup time to UTP_CLK	10	NA	NA	ns
t_2	UTP_RX_CLAV hold time from UTP_CLK	1	NA	NA	ns
t_3	UTP_CLK to UTP_RX_EN	1	NA	NA	ns
t_4	UTP_RX_SOC setup time to UTP_CLK	10	NA	NA	ns
t_5	UTP_RX_SOChold time from UTP_CLK	1	NA	NA	ns
t_6	UTP_RX_DATA setup time to UTP_CLK	10	NA	NA	ns
t_7	UTP_RX_DATA hold time from UTP_CLK	1	NA	NA	ns

Figure 2-11 UTOPIA Receive



2.2.5 DDR Interface

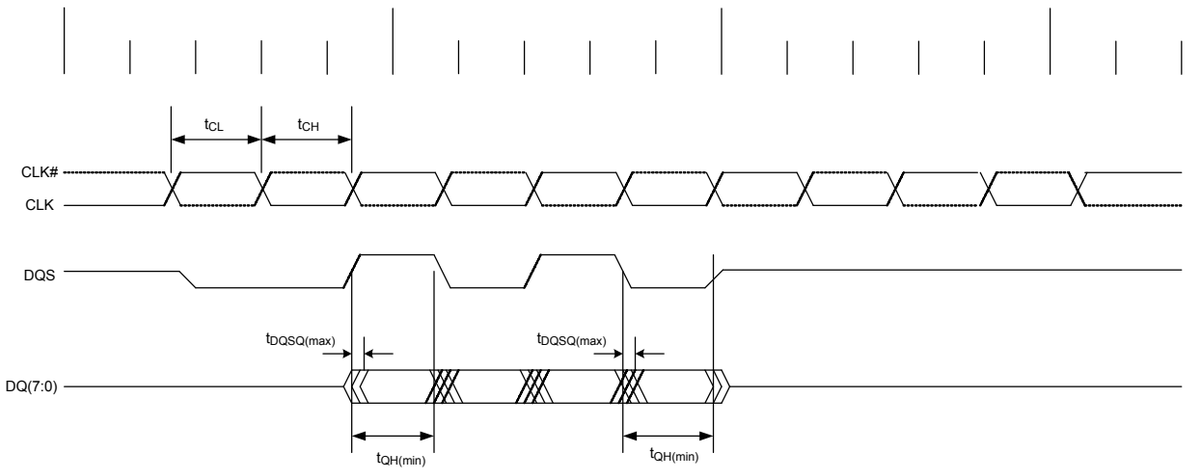
Table 2-18 DDR 200 Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_{RCD}	RAS to READ or WRITE command	20			ns
t_{RP}	RAS precharge	20			ns
t_{RC}	RAS cycle time	70			ns
t_{REFI}	Average Periodic Refresh Interval 64, 128MB			15.6	?s
t_{REFI}	Average Periodic Refresh Interval 256, 512MB, 1GB			7.8	?s
t_{RFC}	Auto Refresh to Active/Auto Refresh command period for 64, 128, 256, 512MB	80			ns
t_{RFC}	Auto Refresh to Active/Auto Refresh command period for 1GB	140			ns
t_{CL}	CK low-level width	0.45		0.55	t_{CK}
t_{CH}	CK high-level width	0.45		0.55	t_{CK}
$t_{SL(I)}$	Input Slew Rate (for input only pins)	0.5			V/ns
$t_{SL(IO)}$	Input Slew Rate (for I/O pins)	0.5			V/ns
$t_{SL(O)}$	Output Slew Rate (x4, x8)	1.0		4.5	V/ns
$t_{SL(O)}$	Output Slew Rate (x16)	0.7		5.0	V/ns
t_{SLMR}	Output Slew Rate Matching Ratio (rise to fall)	0.67		1.5	
t_{RAP}	RAS to READ (with AUTO PRECHARGE) for devices not supporting t_{RAS} lockout	50 – BL * t_{CK}/2			ns
t_{RAP}	RAS to READ (with AUTO PRECHARGE) for devices supporting t_{RAS} lockout	20			ns
t_{IH}	Address and Control input hold time	1.1			ns
t_{IS}	Address and Control input setup time	1.1			ns
t_{DQSS}	Write Command to first DQS latching transition	0.75		1.25	t_{CK}
t_{DH}	DQ and DM input hold time	0.6			ns
t_{DS}	DQ and DM input setup time	0.6			ns
t_{DQSQ}	DQS-DQ Skew (for DQS and associated DQ signals) Skew from DQS to last DQ (7:0)	NA		0.6	ns
t_{HP}	Half Period = minimum of actual (t_{CH}, t_{CL})	45% t_{CK}		NA	t_{CK}
t_{QH}	Data Hold from DQS to earliest DQ (7:0) next clock edge	t_{HP} - t_{QHS}		NA	ns
t_{QHS}	Data Hold Skew	NA		1	ns
t_{RR}	Refresh to Refresh Period 64, 128MB			140	?s
t_{RR}	Refresh to Refresh Period 256, 512MB, 1GB			70	?s
t_{PDN}	Power Down Duration (CKE negated) 64, 128MB			140	?s
t_{PDN}	Power Down Duration (CKE negated) 256, 512MB, 1GB			70	?s
t_{XPDN}	Power Down Exit (Note – exit to read, write and activate)	10			ns

Symbol	Parameter	Min	Typ	Max	Unit
t_{CK}	Clock Cycle Time	10		12	ns
t_{MRD}	MODE REGISTER SET command cycle time	20			ns
t_{RRD}	ACTIVE bank A to ACTIVE bank B command	20			ns
t_{HZ}	Data-out high-impedance time from CK/CKN (DQ/DQS)	-1.2		+0.8	ns
t_{LZ}	Data-out low-impedance time from CK/CKN (DQ)	-1.2		+0.8	ns
t_{LZ}	Data-out low-impedance time from CK/CKN (DQS)	-1.1		+0.8	ns
t_{WR}	Write Recovery Time	20			ns
t_{DAL}	Auto Precharge write recovery + precharge time	40			ns
t_{RPST}	Read Postamble	0.4		0.6	t_{CK}
t_{RPRE}	Read Preamble	0.9		1.1	t_{CK}
t_{XSNR}	Exit SELF REFRESH to non-READ command	200			t_{CK}
t_{DQSL}	DQS input low pulse width	0.35			t_{CK}
t_{DQSH}	DQS input high pulse width	0.35			t_{CK}

NOTE: t DQSQ and tQH apply for all relevant strobe edges. tHP = min(tCL, tCH) t(CL,CH) = 0.5 * tCK – tJIT(HP) tJIT(crosstalk) – 0.45 * tCK

Figure 2-12 Data Output (Read)



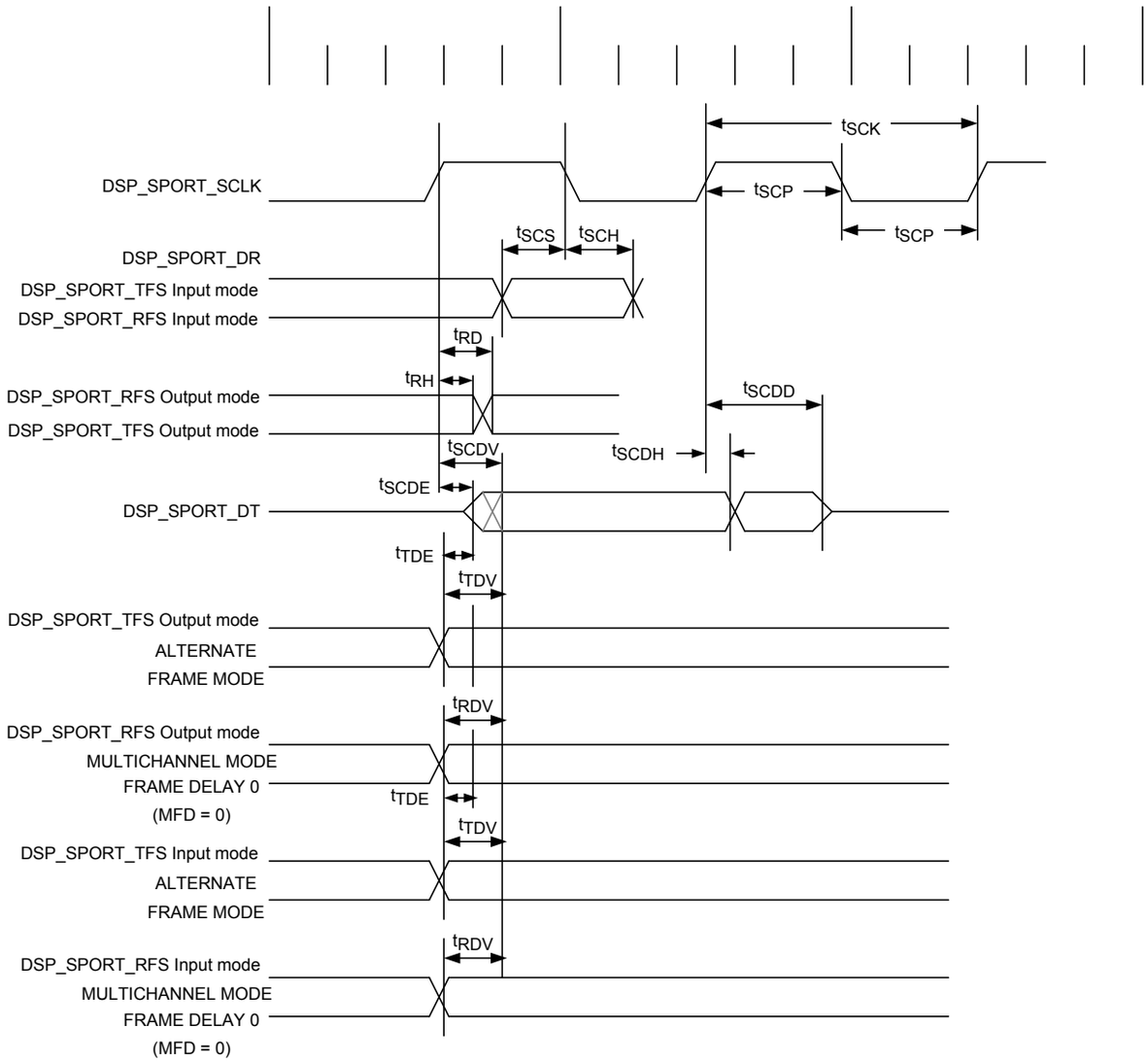
2.2.6 DSP Interface

Table 2-19 DSP SPORT Parameter

Symbol	Parameter	Min	Typ	Max	Unit
Timing Requirements					
t_{SCK}	DSP_SPORT_SCLK period	20	NA	NA	ns
t_{SCS}	DSP_SPORT_DR / DSP_SPORT_TFS / DSP_SPORT_RFS setup before DSP_SPORT_SCLK low	4	NA	NA	ns
t_{SCH}	DSP_SPORT_DR / DSP_SPORT_TFS / DSP_SPORT_RFS hold after DSP_SPORT_SCLK low	7	NA	NA	ns
t_{SCP}	DSP_SPORT_SCLK input width	10	NA	NA	ns
Switching Characteristics					
t_{SCDE}	DSP_SPORT_SCLK high to DSP_SPORT_DT enable	0			ns
t_{SCDV}	DSP_SPORT_SCLK high to DSP_SPORT_DT valid			12	ns
t_{RH}	DSP_SPORT_TFS / DSP_SPORT_RFSOUT hold after DSP_SPORT_SCLK high	0			ns
t_{RD}	DSP_SPORT_TFS / DSP_SPORT_RFSOUT delay from DSP_SPORT_SCLK high			12	ns
t_{SCDH}	DSP_SPORT_DT hold after SCLK high	0			ns
t_{TDE}	DSP_SPORT_TFS (alt) to DSP_SPORT_DT enable	0			ns
t_{TDV}	DSP_SPORT_TFS (alt) to DSP_SPORT_DT valid			12	ns
t_{SCDD}	DSP_SPORT_SCLK high to DSP_SPORT_DT disable			12	ns
t_{RDV}	DSP_SPORT_RFS (multichannel, frame delay zero) to DSP_SPORT_DT valid			12	ns

NOTE: This timing diagram is applicable for SPORT0s and SPORT1s of DSP0 and DSP1; and SPORT 2

Figure 2-13 DSP SPORT



2.2.7 Asynchronous Interface

Figure 2-14 EBIU Asynchronous Read Bus Cycle

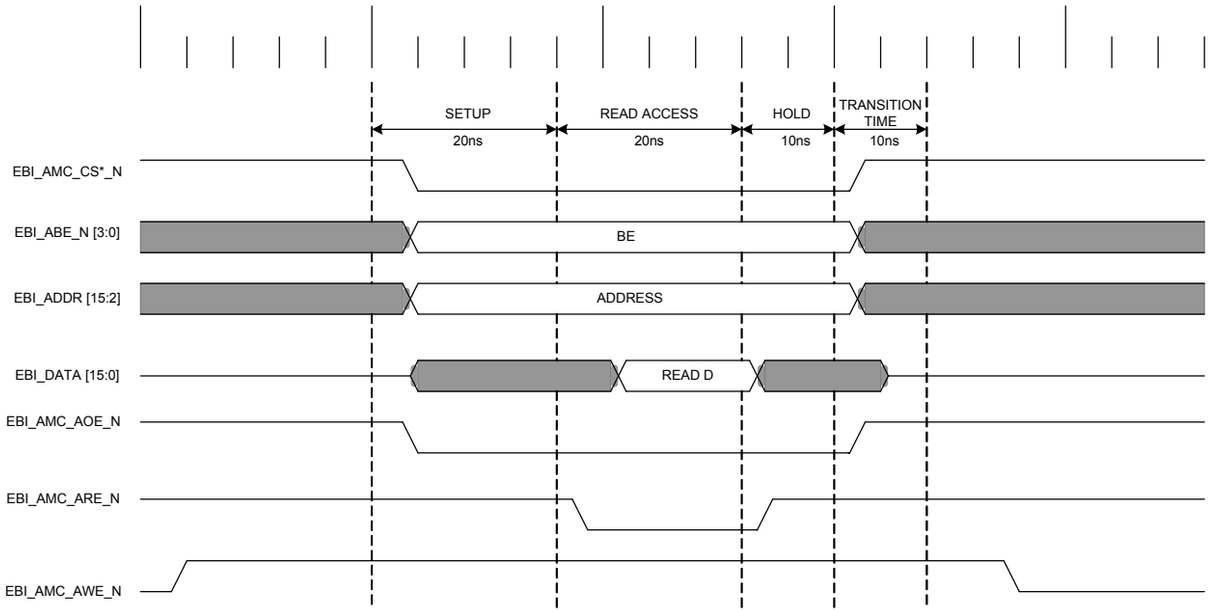


Figure 2-15 EBIU Asynchronous Write and Read Bus Cycle

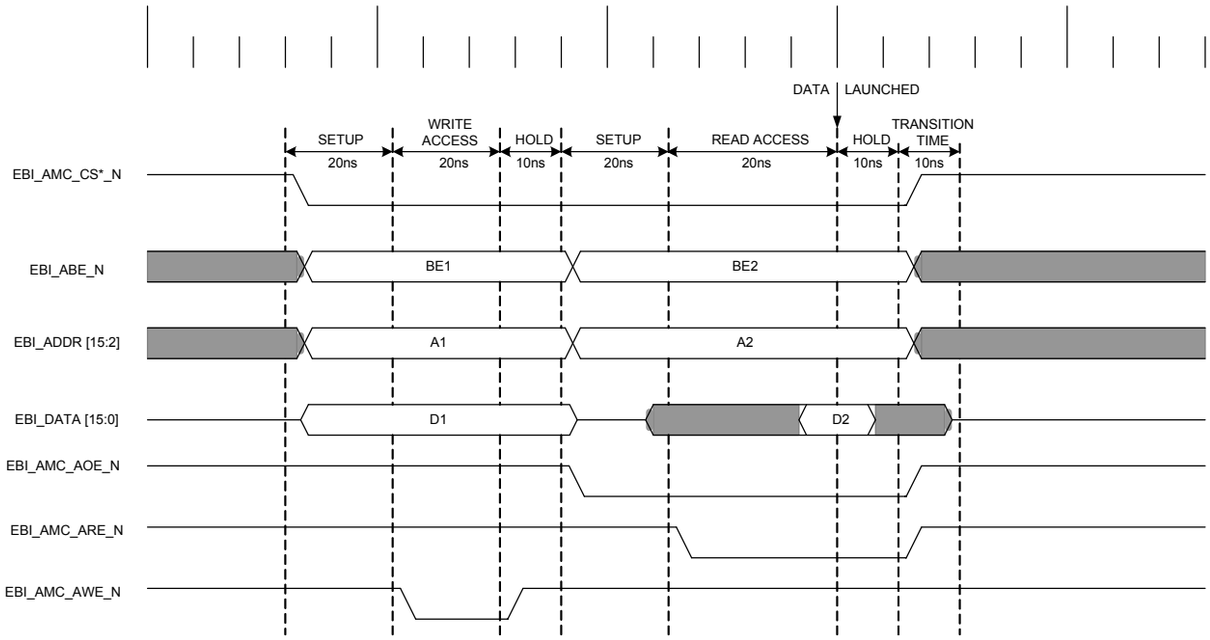
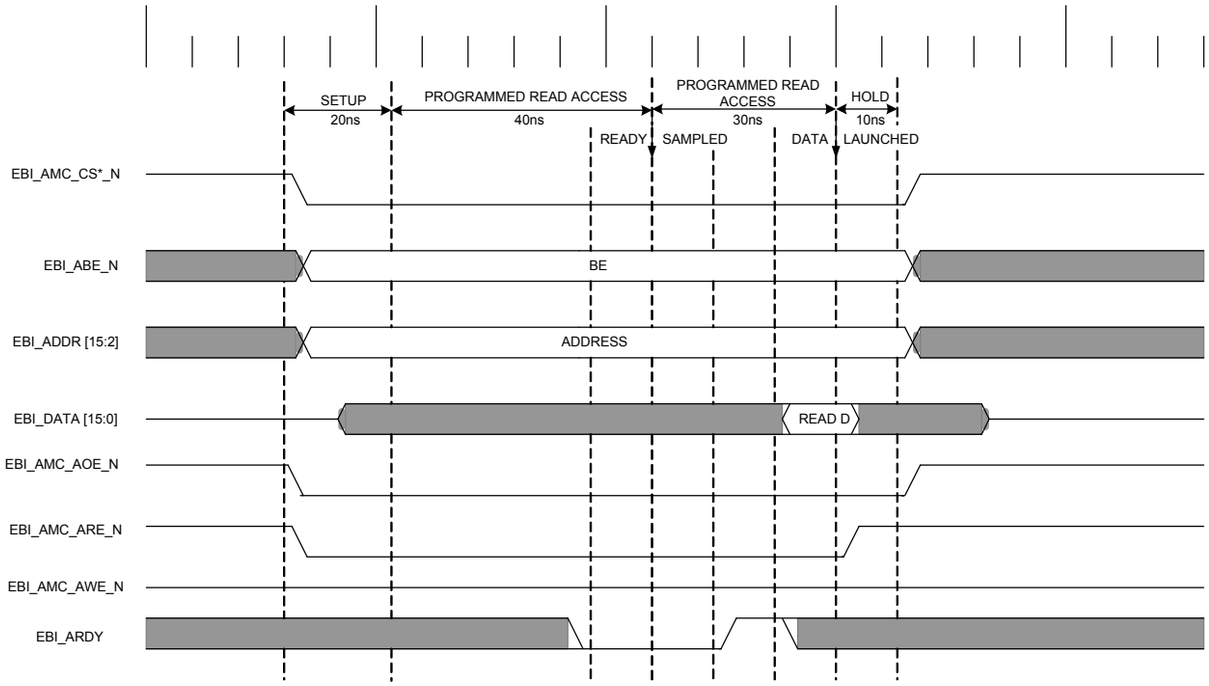


Figure 2-16 EBIU Inserting Wait States Using ARDY

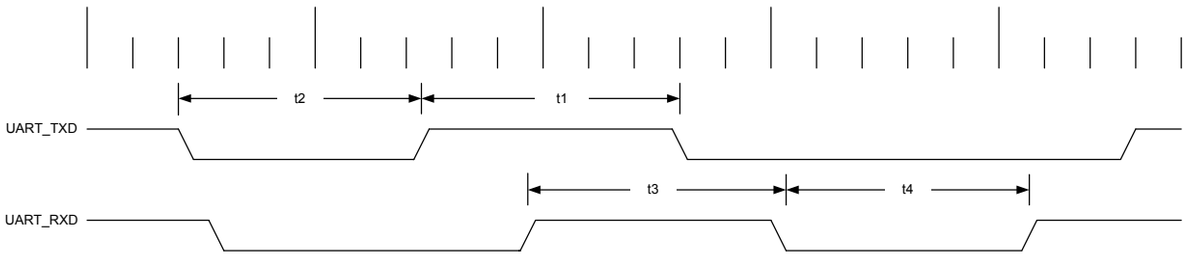


2.2.8 UART 1, 2 Interfaces

Table 2-20 UART 1,2 Parameter (for baud rate 921600)

Symbol	Parameter	Min	Typ	Max	Unit
t_1	UART_TXD high pulse width	1085			ns
t_2	UART_TXD low pulse width	1085			ns
t_3	UART_RXD high pulse width	1085			ns
t_4	UART_RXD low pulse width	1085			ns

Figure 2-17 UART 1,2



2.2.9 AFE (Analog Front End) Interface

The AFE Interface consists of DAC samples (AFE_DAC) clocked out of the data pump 8 bits at 35.328 MHz for an effective rate of 16 bits at 17.664 MHz, and ADC samples (AFE_ADC) clocked in from the AFE 4 bits at 35.328 MHz for an effective rate of 16 bits at 8.832 MHz. a sync signal, AFE_SYNCOUT, is used to denote the Most Significant Bits of the words being transferred in each direction. The AFE_MCLK is an output clock generated to operate the AFE chip.

Figure 2-18 AFE Connections to the CPE AFE

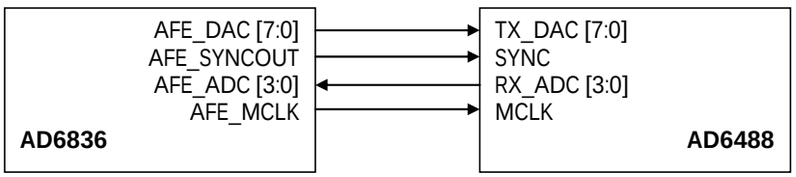


Figure 2-19 AFE Logical Timing

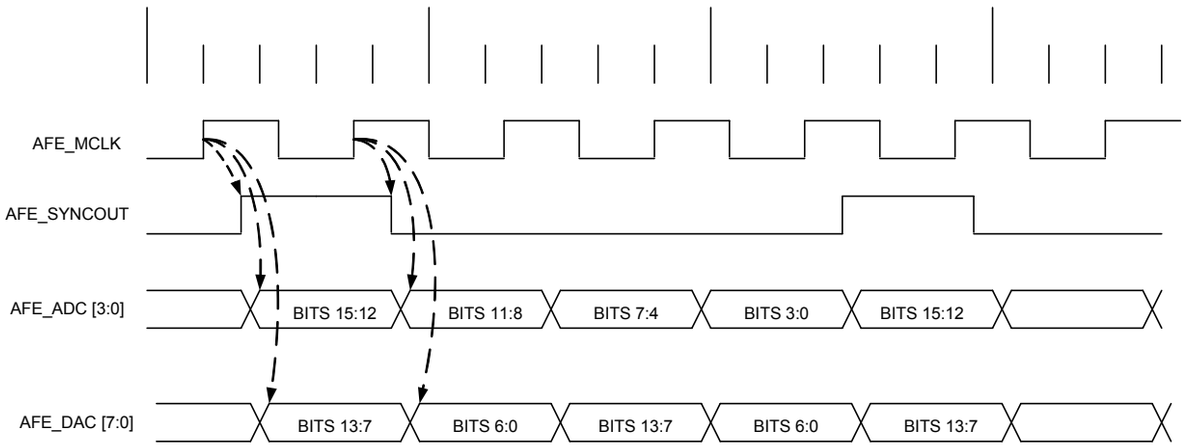


Table 2-21 AFE MCLK Parameter

Symbol	Parameter	Min	Typ	Max	Unit
t_1	AFE_MCLK cycle time	-TBD-	28.31	28.31	ns
t_2	AFE_MCLK high time	11.2			ns
t_3	AFE_MCLK low time	-TBD-			ns
t_4	AFE_MCLK to AFE_SYNCOUT valid	-TBD-			ns
t_5	AFE_MCLK to AFE_DAC valid	-TBD-			ns
t_6	AFE_ADC setup time to AFE_MCLK	-TBD-			ns
t_7	AFE_ADC hold time to AFE_MCLK	-TBD-			ns

Figure 2-20 AFE MCLK

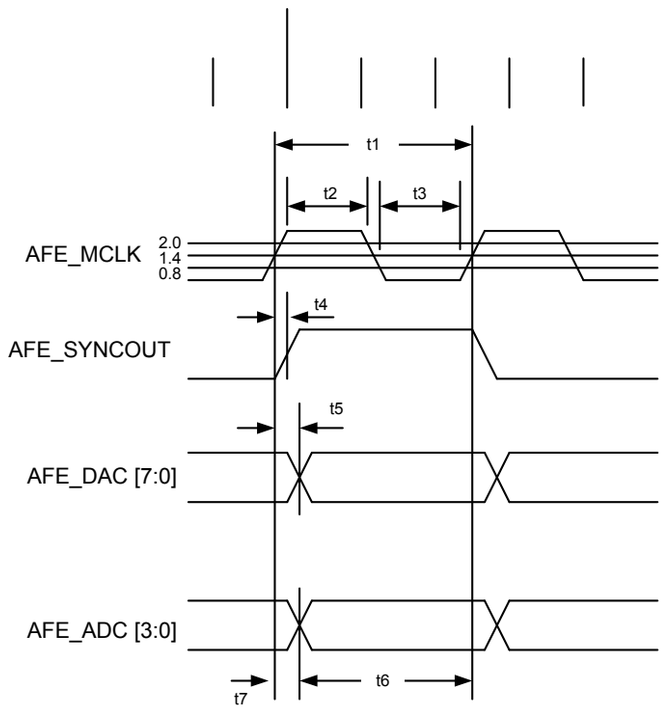
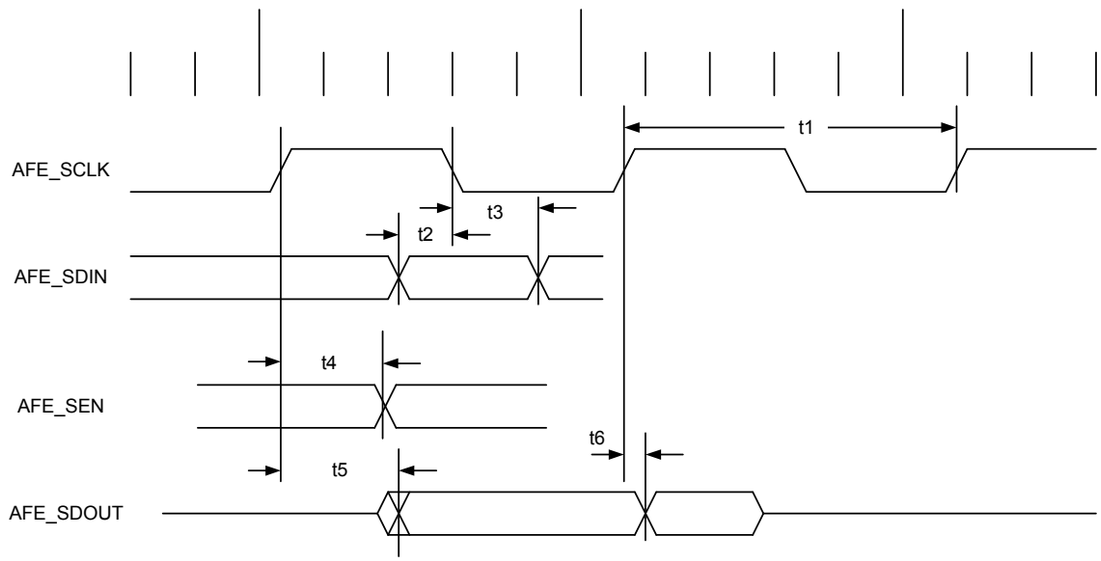


Table 2-22 AFE Serial Port

Symbol	Parameter	Min	Typ	Max	Unit
t_1	AFE_SCLK cycle time		76		ns
t_2	AFE_SDIN Setup before AFE_SCLK Low	10			ns
t_3	AFE_SDIN Hold after AFE_SCLK Low	10			ns
t_4	AFE_SEN Delay after AFE_SCLK High	0		12	ns
t_5	AFE_SDOUT Delay after AFE_SCLK High	0		12	ns

Figure 2-21 AFE Serial Interface



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3 Pin Descriptions

Table 3-1 Glossary of Directional Terms

I	Input
O	Output
IPU	Input; Internal Pull Up
IPD	Input; Internal Pull Down
I/O	Input/Output
I/OPU	Input/Output; Internal Pull Up
I/OPD	Input/Output; Internal Pull Down
_N	Active Logic Low, else High (default)

Table 3-2 PU. PD Resistor Values

Resistor	Min	Typ	Max
PU	32KΩ	45 KΩ	75 KΩ
PD	24 KΩ	42 KΩ	87 KΩ

3.1 Pin Grouping by Function

Table 3-3 I/O Signal Descriptions

Pin	Pin Name	Signal Direction	Pad Direction	Description
IKF6836 Control				
A20	PWR_RESET_N	I	I	Power on Reset, Asynchronous Active Low, must be low for at least 2 µs. Resets the device.
B6	TESTMODE	I	IPD	Enables ATPG scan test mode.
A21	ETH_PHY_CLK	O	I/O	25 MHz Ethernet PHY Clock Output
B15	XTAL_35_XIN	I	-	35.328 MHz Resonator (crystal) connection for ADSL2plus and DSP
A15	XTAL_35_XOUT	O	-	35.328 MHz Resonator (crystal) connection for ADSL2plus and DSP

Pin	Pin Name	Signal Direction	Pad Direction	Description
D21	XTAL_25_XIN	I	-	25 MHz Resonator (crystal) connection for the System
D22	XTAL_25_XOUT	O	-	25 MHz Resonator (crystal) connection for the System
B16	XTAL_UTMI_XIN	I	-	12 MHz Resonator (crystal) connection for UTMI
A16	XTAL_UTMI_XOUT	O	-	12 MHz Resonator (crystal) connection for UTMI
JTAG Interface				
C6	JTG_TCLK	I	IPD	JTAG Test Clock
E7	JTG_TDI	I	IPU	JTAG Test Data In
E6	JTG_TDO	O	O	JTAG Test Data Out
D6	JTG_TMS	I	IPU	JTAG Test Mode Select
D7	JTG_TRST_N	I	IPU	JTAG Test Reset. Active Low
AFE Interface				
U21	AFE_MCLK	I/O	I/O	Analog Front End Clock with a frequency of 35.328 MHz
U20	AFE_SYNCOUT	O	I/OPD	Synchronization Input on the AFE interface for sending data synchronously to AFE_SCLK
See table_a	AFE_DAC [7:0]	O	See table_a	AFE Digital to Analog Data
U19, U18, V19, V20	AFE_ADC [3:0]	I	I/OPD	AFE Analog to Digital Data
W21	AFE_SCLK	O	O	AFE Serial Clock Output
W22	AFE_SDOUT	O	O	AFE Serial Data Out
V21	AFE_SDIN	I	I/OPD	AFE Serial Data In
V22	AFE_SEN	O	I/OPD	Serial Control Port Active (0 = active)
AMC Interface				
See table_b	AMC_DATA [15:0]	I/O	See table_b	AMC Data Bus Pins [15:0]
See table_c	AMC_ADDR [23:2]	O	See table_c	AMC Address Pins [23:2]
C4	AMC_ARDY	I	IPD	Wait State signal from external devices
See table_d	AMC_CS_N [3:0]	O	See table_d	Asynchronous/FLASH Memory Chip Select Pins [3:0]. Active Low
A2	AMC_AOE_N	O	O	Asynchronous/FLASH Memory Output Enable. Active Low
C5	AMC_AWE_N	O	O	Asynchronous Memory Write Enable. Active Low
B5	AMC_ARE_N	O	O	Asynchronous Memory Read Enable. Active Low
A6, A5	AMC_ABE_N [3:2]	O	O	Byte Enables for Async Memory. Active Low

Pin	Pin Name	Signal Direction	Pad Direction	Description
DDR Interface				
See table_f	DDR_DATA [15:0]	I/O	I/O	DDR Data Bus Pins [15:0]
See table_g	DDR_ADDR [12:0]	O	O	DDR Address Pins [12:0]
U4, U3	DDR_BA [1:0]	O	O	DDR Bank Address Pins [1:0]
U2, U1	DDR_CS_N [1:0]	O	O	DDR Chip Select Pins [1:0]. Active Low
P1	DDR_SCLK	O	O	DDR Clock
N1	DDR_SCLK_N	O	O	Inverted DDR Clock
P3	DDR_CLKE	O	O	DDR Clock Enable
M4, N4	DDR_DQS [1:0]	I/O	I/O	DDR Data Strobe Pins [1:0]
N3, N2	DDR_DQM [1:0]	O	O	DDR Data Mask Pins [1:0]
V4	DDR_SWE_N	O	O	DDR Write Enable. Active Low
V2	DDR_SRAS_N	O	O	DDR Row Address Select. Active Low
V3	DDR_SCAS_N	O	O	DDR Column Address Select. Active Low
MII 1 Interface				
H19, H18, G18, G19	MII_1_TX_DATA [3:0]	O	I/OPD	MII Transmit Data Pins [3:0] to PHY Device
G20	MII_1_TX_EN	O	I/OPD	MII Transmit Data Enable
G21	MII_1_TX_CLK	I	IPD	MII Transmit Clock from PHY Device
E15, F18, F19, F20	MII_1_RX_DATA [3:0]	I	I/OPD	MII Receive Data Pins [3:0] from PHY Device
F21	MII_1_RX_EN	I	I/OPD	MII Receive Data Enable
F22	MII_1_RX_CLK	I	IPD	MII Receive Clock from PHY Device
G22	MII_1_RX_ERR	I	I/OPD	MII Receive Error
H21	MII_1_CAR_SENSE	I	I/OPD	MII Carrier Sense Detect
H20	MII_1_COL_DET	I	I/OPD	MII Collision Detect
MII 2 Interface				
See table_e	MII_2_TX_DATA [3:0]	O	See table_e	MII Transmit Data Pins [3:0] to PHY Device
C12	MII_2_TX_EN	O	I/OPD	MII Transmit Data Enable
B12	MII_2_TX_CLK	I	I	MII Transmit Clock from PHY Device
C9, B9, A9, A10	MII_2_RX_DATA [3:0]	I	IPU	MII Receive Data Pins [3:0] from PHY Device
B10	MII_2_RX_EN	I	IPD	MII Receive Data Enable
C10	MII_2_RX_CLK	I	I	MII Receive Clock from PHY Device
B11	MII_2_RX_ERR	I	IPD	MII Receive Error
C14	MII_2_CAR_SENSE	I	IPD	MII Carrier Sense Detect

Pin	Pin Name	Signal Direction	Pad Direction	Description
B14	MII_2_COL_DET	I	IPD	MII Collision Detect
MII PHY Management Interface				
E14	MDI_CLK	O	O	Media Interface Management Clock. Maximum value is 2.5MHz
D14	MDI_DATA	I/O	I/OPD	Management Data to and from PHY Devices
UART 1				
B8	URT_1_RXD	I	IPD	UART 1 Receive Data
C8	URT_1_TXD	O	O	UART 1 Transmit Data
UART 2				
E8	URT_2_RXD	I	I/OPD	UART 2 Receive Data
D8	URT_2_TXD	O	I/OPD	UART 2 Transmit Data
E9	URT_2_CTS	I	I/OPD	UART 2 Clear To Send
D9	URT_2_RTS	O	I/OPD	UART 2 Request To Send
UTOPIA				
K18	UTP_ CLK	O	O	UTOPIA Transmit/Receive Clock, 25 – 33 MHz
See table_h	UTP_TX_DATA [7:0]	O	O	UTOPIA Transmit Data Pins [7:0] to a Slave Device
R20	UTP_TX_PRTY	O	O	UTOPIA Transmit Parity
H22	UTP_TX_SOC	O	O	UTOPIA Transmit Start of Cell
J21	UTP_TX_EN_N	O	O	UTOPIA Transmit Data Enable. Active Low
J18, J19, J20	UTP_TX_ADDR [2:0]	O	O	UTOPIA Transmit Address Pins [2:0], Slave device identifier
J22	UTP_TX_CLAV	I	I	UTOPIA Transmit Cell Available
See table_i	UTP_RX_DATA [7:0]	I	I/OPD	UTOPIA Receive Data Pins [7:0] from Slave Device
R21	UTP_RX_PRTY	I	I	UTOPIA Receive Parity
R22	UTP_RX_SOC	I	I	UTOPIA Receive Start of Cell
P21	UTP_RX_EN_N	O	O	UTOPIA Receive Data Enable. Active Low
P18, P19, P20	UTP_RX_ADDR [2:0]	O	O	UTOPIA Receive Address Pins [2:0], Slave device identifier
P22	UTP_RX_CLAV	I	I	UTOPIA Receive Cell Available
Serial Peripheral Interface (Master Mode)				
W19	SPI_ERROR	I	I/OPU	Error Input
Y19	SPI_CS1_OUT	O	I/OPU	Chip Select 1 Out for selecting Slave 1
AA19	SPI_CS2_OUT	O	I/OPD	Chip Select 2 Out for selecting Slave 2

Pin	Pin Name	Signal Direction	Pad Direction	Description
V18	SPI_SDATA	I	I/OPD	Serial Peripheral Interface Data In
W18	SPI_MDATA	O	I/OPD	Serial Peripheral Interface Data Out
Y18	SPI_CLK	O	I/OPD	Serial Peripheral Interface Clock, programmable. Max. up to 25 MHz
Serial Peripheral Interface (Slave Mode)				
W19	SPI_CS	I	I/OPU	Chip Select
V18	SPI_SDATA	O	I/OPD	Serial Peripheral Interface Data Out
W18	SPI_MDATA	I	I/OPD	Serial Peripheral Interface Data In
Y18	SPI_CLK	I	I/OPD	Serial Peripheral Interface Clock, programmable. Max. up to 25 MHz
PCI				
AA17	PCI_CLK_I	I	I	PCI Clock input, 33.33 MHz
AA18	PCI_CLK_O	O	O	PCI Clock output, 33.33 MHz
AB17	PCI_RST_N	I/O	I/O	PCI Reset, Active Low
Y16	PCI_EXT_1_REQ_N	I	I	Request from external device 1 (when Fusiv-VX 160 is a central resource). Active Low
V17	PCI_EXT_1_GNT_N	O	O	Grant to external device 1 (when Fusiv-VX 160 is a central resource). Active Low
W16	PCI_EXT_2_REQ_N	I	I	Request from external device 2 (when Fusiv-VX 160 is a central resource). Active Low
V16	PCI_EXT_2_GNT_N	O	O	Grant to external device 2 (when Fusiv-VX 160 is a central resource). Active Low
W17	PCI_EXT_3_REQ_N / PCI_GNT_N	I	I	Request from external device 3 (when Fusiv-VX 160 is a central resource) / PCI Bus Grant (when Fusiv-VX 160 is not a central resource). Active Low
AA16	PCI_EXT_3_GNT_N / PCI_REQ_N	O	O	Grant to external device 3 (when Fusiv-VX 160 is a central resource) / PCI Bus Request (when Fusiv-VX 160 is not a central resource). Active Low
AB14	PCI_IDSEL_N	I	I	PCI ID Select
W10	PCI_TRDY_N	I/O	I/O	PCI Target Ready. Active Low
Y10	PCI_DEVSEL_N	I/O	I/O	PCI Device Select. Active Low
AA10	PCI_STOP_N	I/O	I/O	PCI Stop. Active Low
AA11	PCI_FRAME_N	I/O	I/O	PCI Frame
AB10	PCI_LOCK_N	I	I	PCI Lock. Active Low
AB9	PCI_PERR_N	I/O	I/O	PCI Parity Error. Active Low
AA9	PCI_SERR_N	I/O	I/O	PCI System Error. Active Low

Pin	Pin Name	Signal Direction	Pad Direction	Description
AA14, AB11, W9, Y7	PCI_CBE_N [3:0]	I/O	I/O	PCI Command and Byte Enables. Active Low
Y9	PCI_PAR	I/O	I/O	PCI Parity Signal
Y17	PCI_INTA_N	I/O	I/O	PCI Interrupt. Active Low
AA15	PCI_PME_N	O	I/O	PCI Power Management Enable. Active Low
See table_j	PCI_AD [31:0]	I/O	I/O	PCI Address/Data Bus Pins [31:0]
Y11	PCI_IRDY_N	I/O	I/O	PCI Initiator Ready. Active Low
W11	PCI_CLKRUN_N	I/O	I/O	PCI Clock Run
USB 2.0 FS Device				
A19	USBD_DPLUS	I/O	I/O	USB FS Differential Data In, D+, receive from the transceiver
A18	USBD_DMINUS	I/O	I/O	USB FS Differential Data In, D -, receive from the transceiver
USB 2.0 HS/FS/LS Host				
A12	USBH_DPLUS	I/O	I/O	USB HS/FS/LS Differential Data In, D+, receive from the transceiver
A11	USBH_DMINUS	I/O	I/O	USB HS/FS/LS Differential Data In, D -, receive from the transceiver
C11	USBH_RREFEXT	I/O	I/O	External resistor connection for current reference.
GPIO				
See table_k	GPIO [31:0]	I/O	See table_k	General Purpose IO Pins [31:0]
DSP 0 Interface				
W20	DSP0_SPORT0_DR	I	I	Serial Port 0 Receive Data
Y22	DSP0_SPORT0_DT	O	O	Serial Port 0 Transmit Data
Y21	DSP0_SPORT0_RFS	I/O	I/O	Serial Port 0 Receive Frame Sync
AA22	DSP0_SPORT0_TFS	I/O	I/O	Serial Port 0 Transmit Frame Sync
AB21	DSP0_SPORT0_SCLK	I/O	I/O	Serial Port 0 Clock
AB4	DSP0_SPORT1_DR	I	I	Serial Port 0 Receive Data
AB2	DSP0_SPORT1_DT	O	O	Serial Port 0 Transmit Data
AB3	DSP0_SPORT1_RFS	I/O	I/O	Serial Port 0 Receive Frame Sync
AA1	DSP0_SPORT1_TFS	I/O	I/O	Serial Port 0 Transmit Frame Sync
AA2	DSP0_SPORT1_SCLK	I/O	I/O	Serial Port 0 Clock
AB19	DSP0_PF2	I/O	I/OPD	Programmable Flag 2
AB20	DSP0_PF3	I/O	I/OPD	Programmable Flag 3

Pin	Pin Name	Signal Direction	Pad Direction	Description
AB5	DSP0_EE	I	I/O	DSP0 Emulator Enable
AB6	DSP0_EBR_N	I	I/O	DSP0 Emulator Bus Request. Active Low
AA6	DSP0_EBG_N	O	I/O	DSP0 Emulator Bus Grant. Active Low
Y6	DSP0_ERESET_N	I	I/O	DSP0 Emulator Controlled Reset. Active Low
W6	DSP0_EMS_N	O	I/O	DSP0 Emulator Memory Select. Active Low
V6	DSP0_EINT_N	I	I/O	DSP0 Emulator Interrupt Pin. Active Low
V7	DSP0_ECLK	I	I/O	DSP0 Emulator Clock (16.67 MHz)
W7	DSP0_ELIN	I	I/O	DSP0 Emulator Data In
AA7	DSP0_ELOUT	O	I/O	DSP0 Emulator Data Out
DSP 1 Interface				
W20	DSP1_SPORT0_DR	I	I	Serial Port 0 Receive Data
Y22	DSP1_SPORT0_DT	O	O	Serial Port 0 Transmit Data
Y21	DSP1_SPORT0_RFS	I/O	I/O	Serial Port 0 Receive Frame Sync
AA22	DSP1_SPORT0_TFS	I/O	I/O	Serial Port 0 Transmit Frame Sync
AB21	DSP1_SPORT0_SCLK	I/O	I/O	Serial Port 0 Clock
AB4	DSP1_SPORT1_DR	I	I	Serial Port 1 Receive Data
AB2	DSP1_SPORT1_DT	O	O	Serial Port 1 Transmit Data
AB3	DSP1_SPORT1_RFS	I/O	I/O	Serial Port 1 Receive Frame Sync
AA1	DSP1_SPORT1_TFS	I/O	I/O	Serial Port 1 Transmit Frame Sync
AA2	DSP1_SPORT1_SCLK	I/O	I/O	Serial Port 1 Clock
AA20	DSP1_PF2	I/O	I/OPD	Programmable Flag 2
Y20	DSP1_PF3	I/O	I/OPD	Programmable Flag 3
AB7	DSP1_EE	I	I/O	DSP1 Emulator Enable
AB8	DSP1_EBR_N	I	I/O	DSP1 Emulator Bus Request. Active Low
AA8	DSP1_EBG_N	O	I/O	DSP1 Emulator Bus Grant. Active Low
Y8	DSP1_ERESET_N	I	I/O	DSP1 Emulator Controlled Reset. Active Low
W8	DSP1_EMS_N	O	I/O	DSP1 Emulator Memory Select. Active Low
V8	DSP1_EINT_N	I	I/O	DSP1 Emulator Interrupt Pin. Active Low
V9	DSP1_ECLK	I	I/O	DSP1 Emulator Clock (16.67 MHz)
AB12	DSP1_ELIN	I	I/O	DSP1 Emulator Data In
AA12	DSP1_ELOUT	O	I/O	DSP1 Emulator Data Out
SPORT on System Bus				
Y4	SPORT2_TSCLK	I/O	I/OPD	Serial Clock for Transmit path
Y3	SPORT2_RSCLK	I/O	I/OPD	Serial Clock for Receive path

Pin	Pin Name	Signal Direction	Pad Direction	Description
Y5	SPORT2_TFS	I/O	I/OPD	Transmit Frame Sync
AA4	SPORT2_RFS	I/O	I/OPD	Receive Frame Sync
AA5	SPORT2_DT	O	O	Transmit Data
AA3	SPORT2_DR	I	IPD	Receive Data
EJTAG PCTRACE Interface				
Y11	EJTAG_DCLK	O	I/O	EJTAG DCLK
W12, Y12	EJTAG_TPC [2:1]	O	I/O	EJTAG Trace PC Pins [2:1]
See table 1	EJTAG_PCST [11:0]	O	I/O	EJTAG PC Status Pins [11:0]
Control Power & Ground				
V1	SSTL2_RREFGEN_1.25V	-	-	1.25V reference input voltage for SSTL2 pads
D15	XTAL_35_1.8	-	-	35.328 MHz Crystal Power pad
C15	XTAL_35_GND	-	-	35.328 MHz Crystal Ground
D20	XTAL_25_1.8	-	-	25 MHz Crystal Power pad
E22	XTAL_25_GND	-	-	25 MHz Crystal Ground
E16	XTAL_UTMI_1.8	-	-	UTMI Crystal Power pad
D16	XTAL_UTMI_GND	-	-	UTMI Crystal Ground
USB (Device, Host) Power & Ground				
B20	USBD_3.3_A	-	-	USB Device Analog Power
B19	USBD_GND_A	-	-	USB Device Analog Ground
D10	USBH_3.3_A	-	-	USB Host Analog Power
B13	USBH_GND_A	-	-	USB Host Analog Ground
C13	USBH_1.8_P	-	-	USB Host PLL Power
D11	USBH_GND_P	-	-	USB Host PLL Ground
PLL Power & Ground				
A17	PLL_SPHY_1.8_D	-	-	ADSL PLL Digital Power pad
C17	PLL_SPHY_1.8_A	-	-	ADSL PLL Analog Power pad
C16	PLL_SPHY_GND_D	-	-	ADSL PLL Digital Ground
B17	PLL_SPHY_GND_A	-	-	ADSL PLL Analog Ground
C22	PLL_USB_1.8_D	-	-	USB PLL Digital Power pad
B21	PLL_USB_1.8_A	-	-	USB PLL Analog Power pad
C21	PLL_USB_GND_D	-	-	USB PLL Digital Ground
B22	PLL_USB_GND_A	-	-	USB PLL Analog Ground
C18	PLL_DSP_1.8_D	-	-	DSP PLL Digital Power pad

Pin	Pin Name	Signal Direction	Pad Direction	Description
D17	PLL_DSP_1.8_A	-	-	DSP PLL Analog Power pad
B18	PLL_DSP_GND_D	-	-	DSP PLL Digital Ground
E17	PLL_DSP_GND_A	-	-	DSP PLL Analog Ground
D18	PLL_PCI_1.8_D	-	-	PCI PLL Digital Power pad
C20	PLL_PCI_1.8_A	-	-	PCI PLL Analog Power pad
D19	PLL_PCI_GND_D	-	-	PCI PLL Digital Ground
C19	PLL_PCI_GND_A	-	-	PCI PLL Analog Ground
E19	PLL_PROC_1.8_D	-	-	Processor PLL Digital Power pad
E21	PLL_PROC_1.8_A	-	-	Processor PLL Analog Power pad
E18	PLL_PROC_GND_D	-	-	Processor PLL Digital Ground
E20	PLL_PROC_GND_A	-	-	Processor PLL Analog Ground
Core & I/O Power Pins				
21 Pins	1.8V Core	F7, F10, F11, F12, F15, F16, H6, J6, J17, K17, L17, M6, N6, P6, P17, R17, U8, U9, U10, U14, U15		
5 Pins	2.5V IO	K6, L6, R6, T6, U6		
18 Pins	3.3V IO	F6, F8, F9, F13, F14, F17, G6, G17, H17, M17, N17, T17, U7, U11, U12, U13, U16, U1		
Ground Pins				
84 Pins	Ground	A1, A22, E10, E11, E12, E13, H8, H9, H10, H11, H12, H13, H14, H15, J8, J9, J10, J11, J12, J13, J14, J15, K5, K8, K9, K10, K11, K12, K13, K14, K15, L5, L8, L9, L10, L11, L12, L13, L14, L15, L18, M5, M8, M9, M10, M11, M12, M13, M14, M15, M18, N5, N8, N9, N10, N11, N12, N13, N14, N15, N18, P2, P8, P9, P10, P11, P12, P13, P14, P15, R8, R9, R10, R11, R12, R13, R14, R15, V10, V11, V12, V13, AB1, AB22		
NC Pins				
1 Pin	Not Connected	AB18		

Table a. AFE_DAC[7:0]

7	6	5	4	3	2	1	0
R19	R18	T18	T19	T20	T21	T22	U22
I/OPD	I/OPD	I/OPU	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD

Table b. AMC_DATA[15:0]

15	14	13	12	11	10	9	8
F1	E1	E2	E3	E4	E5	D5	D4
I/OPD	I/O	I/OPD	I/OPD	I/OPU	I/OPU	I/OPD	I/OPU

7	6	5	4	3	2	1	0
D3	D2	D1	C1	C2	C3	B2	B1
I/OPD	I/OPU	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD

Table c. AMC_ADDR[23:2]

23	22	21	20	19	18	17	16
F2	F3	F4	F5	G5	G4	G3	G2
O	O	O	O	O	O	O	O

15	14	13	12	11	10	9	8
G1	H1	H2	H3	H4	H5	J5	J4
O	O	O	O	O	I/OPD	I/OPD	I/OPD

7	6	5	4	3	2
J3	J2	J1	K1	K2	K3
I/OPD	I/OPD	O	O	O	O

Table d. AMC_CS_N[3:0]

3	2	1	0
B4	A4	A3	B3
O	O	I/O	I/O

Table e. MII2_TX_DATA[3:0]

3	2	1	0
A14	A13	D13	D12
O	I/OPD	I/OPD	I/OPD

Table f. DDR_DATA[15:0]

15	14	13	12	11	10	9	8
K4	L4	L3	L2	L1	M1	M2	M3

7	6	5	4	3	2	1	0
V5	W5	W4	W3	W2	W1	Y1	Y2

Table g. DDR_ADDR[12:0]

12	11	10	9	8	7	6	5
P4	P5	U5	R5	R4	R3	R2	R1

4	3	2	1	0
T1	T2	T3	T4	T5

Table h. UTP_TX_DATA[7:0]

7	6	5	4	3	2	1	0
L19	L20	L21	L22	K22	K21	K20	K19

Table i. UTP_RX_DATA[7:0]

7	6	5	4	3	2	1	0
M19	M20	M21	M22	N22	N21	N20	N19

Table j. PCI_AD[31:0]

31	30	29	28	27	26	25	24
AB16	AB15	Y15	W15	V15	V14	W14	Y14

23	22	21	20	19	18	17	16
AB13	AA13	Y13	W13	W12	Y12	AA12	AB12

15	14	13	12	11	10	9	8
V9	V8	W8	Y8	AA8	AB8	AB7	AA7

7	6	5	4	3	2	1	0
W7	V7	V6	W6	Y6	AA6	AB6	AB5

Table k. GPIO[31:0]

31	30	29	28	27	26	25	24
A8	A7	B7	C7	AA4	Y5	Y3	Y4
I/OPD	I/OPD	I/O	I/O	I/OPD	I/OPD	I/OPD	I/OPD

23	22	21	20	19	18	17	16
C9	B9	A9	A10	M19	M20	M21	M22
I/OPD	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD

15	14	13	12	11	10	9	8
N22	N21	N20	N19	Y20	AA20	AB20	AB19
I/OPD	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD

7	6	5	4	3	2	1	0
AA21	D9	E9	E8	D8	AA19	Y19	W19
I/OPD	I/OPD	I/OPD	I/OPD	I/OPD	I/OPD	I/OPU	I/OPU

Table l. EJTAG_PCST[11:0]

11	10	9	8	7	6	5	4
AB16	AB15	Y15	W15	V15	V14	W14	Y14

3	2	1	0
AB13	AA13	Y13	W13

3.2 Pin Grouping by Sequence

Table 3-4 IKF6836 Pin List

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
A1	-	GND
A2	O	AMC_AOE_N
A3	I/O	AMC_CS_N_1
A4	O	AMC_CS_N_2
A5	O	AMC_ABE_N_2
A6	O	AMC_ABE_N_3
A7	I/OPD	GPIO_30
A8	I/OPD	GPIO_31
A9	I/OPD	**GPIO_21** / MII_2_RX_DATA_1
A10	I/OPD	**GPIO_20** / MII_2_RX_DATA_0
A11	I/O	USBH_DMINUS
A12	I/O	USBH_DPLUS
A13	I/OPD	MII_2_TX_DATA_2
A14	O	MII_2_TX_DATA_3
A15	-	XTAL_35_XOUT
A16	-	XTAL_UTMI_XOUT
A17	-	PLL_SPHY_1.8_D
A18	I/O	USBD_DMINUS
A19	I/O	USBD_DPLUS
A20	I	PWR_RESET_N
A21	I/O	ETH_PHY_CLK
A22	-	GND
B1	I/OPD	AMC_DATA_0
B2	I/OPD	AMC_DATA_1
B3	I/O	AMC_CS_N_0
B4	O	AMC_CS_N_3
B5	O	AMC_ARE_N
B6	IPD	TESTMODE
B7	I/O	GPIO_29
B8	IPD	URT_1_RXD
B9	I/OPD	**GPIO_22** / MII_2_RX_DATA_2
B10	IPD	MII_2_RX_EN
B11	IPD	MII_2_RX_ERR
B12	I	MII_2_TX_CLK
B13	-	USBH_GND_A
B14	IPD	MII_2_COL_DET
B15	-	XTAL_35_XIN
B16	-	XTAL_UTMI_XIN
B17	-	PLL_SPHY_GND_A
B18	-	PLL_DSP_GND_D
B19	-	USBD_GND_A
B20	-	USBD_3.3_A
B21	-	PLL_USB_1.8_A
B22	-	PLL_USB_GND_A
C1	I/OPD	AMC_DATA_4
C2	I/OPD	AMC_DATA_3
C3	I/OPD	AMC_DATA_2
C4	IPD	AMC_ARDY
C5	O	AMC_AWE_N
C6	IPD	JTG_TCLK
C7	I/O	GPIO_28
C8	O	URT_1_TXD
C9	I/OPD	**GPIO_23** / MII_2_RX_DATA_3
C10	I	MII_2_RX_CLK
C11	I/O	USBH_RREFEXT
C12	I/OPD	MII_2_TX_EN
C13	-	USBH_1.8_P
C14	IPD	MII_2_CAR_SENSE
C15	-	XTAL_35_GND
C16	-	PLL_SPHY_GND_D
C17	-	PLL_SPHY_1.8_A
C18	-	PLL_DSP_1.8_D
C19	-	PLL_PCI_GND_A
C20	-	PLL_PCI_1.8_A
C21	-	PLL_USB_GND_D
C22	-	PLL_USB_1.8_D
D1	I/OPD	AMC_DATA_5
D2	I/OPU	AMC_DATA_6
D3	I/OPD	AMC_DATA_7
D4	I/OPU	AMC_DATA_8
D5	I/OPD	AMC_DATA_9
D6	IPU	JTG_TMS
D7	IPU	JTG_TRST_N
D8	I/OPD	**GPIO_3** / URT_2_TXD
D9	I/OPD	**GPIO_6** / URT_2_RTS
D10	-	USBH_3.3_A
D11	-	USBH_GND_P
D12	I/OPD	MII_2_TX_DATA_0
D13	I/OPD	MII_2_TX_DATA_1
D14	I/OPD	MDI_DATA
D15	-	XTAL_35_1.8
D16	-	XTAL_UTMI_GND
D17	-	PLL_DSP_1.8_A

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
D18	-	PLL_PCI_1.8_D
D19	-	PLL_PCI_GND_D
D20	-	XTAL_25_1.8
D21	-	XTAL_25_XIN
D22	-	XTAL_25_XOUT
E1	I/O	AMC_DATA_14
E2	I/OPD	AMC_DATA_13
E3	I/OPD	AMC_DATA_12
E4	I/OPU	AMC_DATA_11
E5	I/OPU	AMC_DATA_10
E6	O	JTG_TDO
E7	IPU	JTG_TDI
E8	I/OPD	**GPIO_4** / URT_2_RXD
E9	I/OPD	**GPIO_5** / URT_2_CTS
E10	-	GND
E11	-	GND
E12	-	GND
E13	-	GND
E14	O	MDI_CLK
E15	I/OPD	MII_1_RX_DATA3
E16	-	XTAL_UTMI_1.8
E17	-	PLL_DSP_GND_A
E18	-	PLL_PROC_GND_D
E19	-	PLL_PROC_1.8_D
E20	-	PLL_PROC_GND_A
E21	-	PLL_PROC_1.8_A
E22	-	XTAL_25_GND
F1	I/OPD	AMC_DATA_15
F2	O	AMC_ADDR_23
F3	O	AMC_ADDR_22
F4	O	AMC_ADDR_21
F5	O	AMC_ADDR_20
F6	-	3.3V_IO
F7	-	1.8V_CORE

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
F8	-	3.3V_IO
F9	-	3.3V_IO
F10	-	1.8V_CORE
F11	-	1.8V_CORE
F12	-	1.8V_CORE
F13	-	3.3V_IO
F14	-	3.3V_IO
F15	-	1.8V_CORE
F16	-	1.8V_CORE
F17	-	3.3V_IO
F18	I/OPD	MII_1_RX_DATA_2
F19	I/OPD	MII_1_RX_DATA_1
F20	I/OPD	MII_1_RX_DATA_0
F21	I/OPD	MII_1_RX_EN
F22	IPD	MII_1_RX_CLK
G1	O	AMC_ADDR_15
G2	O	AMC_ADDR_16
G3	O	AMC_ADDR_17
G4	O	AMC_ADDR_18
G5	O	AMC_ADDR_19
G6	-	3.3V_IO
G17	-	3.3V_IO
G18	I/OPD	MII_1_TX_DATA_1
G19	I/OPD	MII_1_TX_DATA_0
G20	I/OPD	MII_1_TX_EN
G21	IPD	MII_1_TX_CLK
G22	I/OPD	MII_1_RX_ERR
H1	O	AMC_ADDR_14
H2	O	AMC_ADDR_13
H3	O	AMC_ADDR_12
H4	O	AMC_ADDR_11
H5	I/OPD	AMC_ADDR_10
H6	-	1.8V_CORE
H8	-	GND

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
H9	-	GND
H10	-	GND
H11	-	GND
H12	-	GND
H13	-	GND
H14	-	GND
H15	-	GND
H17	-	3.3V_IO
H18	I/OPD	MII_1_TX_DATA_2
H19	I/OPD	MII_1_TX_DATA_3
H20	I/OPD	MII_1_COL_DET
H21	I/OPD	MII_1_CAR_SENSE
H22	O	UTP_TX_SOC
J1	O	AMC_ADDR_5
J2	I/OPD	AMC_ADDR_6
J3	I/OPD	AMC_ADDR_7
J4	I/OPD	AMC_ADDR_8
J5	I/OPD	AMC_ADDR_9
J6	-	1.8V_CORE
J8	-	GND
J9	-	GND
J10	-	GND
J11	-	GND
J12	-	GND
J13	-	GND
J14	-	GND
J15	-	GND
J17	-	1.8V_CORE
J18	O	UTP_TX_ADDR_2
J19	O	UTP_TX_ADDR_1
J20	O	UTP_TX_ADDR_0
J21	O	UTP_TX_EN_N
J22	I	UTP_TX_CLAV
K1	O	AMC_ADDR_4

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
K2	O	AMC_ADDR_3
K3	O	AMC_ADDR_2
K4	I/O	DDR_DATA_15
K5	-	GND
K6	-	2.5V_IO
K8	-	GND
K9	-	GND
K10	-	GND
K11	-	GND
K12	-	GND
K13	-	GND
K14	-	GND
K15	-	GND
K17	-	1.8V_CORE
K18	O	UTP_CLK
K19	O	UTP_TX_DATA_0
K20	O	UTP_TX_DATA_1
K21	O	UTP_TX_DATA_2
K22	O	UTP_TX_DATA_3
L1	I/O	DDR_DATA_11
L2	I/O	DDR_DATA_12
L3	I/O	DDR_DATA_13
L4	I/O	DDR_DATA_14
L5	-	GND
L6	-	2.5V_IO
L8	-	GND
L9	-	GND
L10	-	GND
L11	-	GND
L12	-	GND
L13	-	GND
L14	-	GND
L15	-	GND
L17	-	1.8V_CORE

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
L18	-	GND
L19	O	UTP_TX_DATA_7
L20	O	UTP_TX_DATA_6
L21	O	UTP_TX_DATA_5
L22	O	UTP_TX_DATA_4
M1	I/O	DDR_DATA_10
M2	I/O	DDR_DATA_9
M3	I/O	DDR_DATA_8
M4	I/O	DDR_DQS_1
M5	-	GND
M6	-	1.8V_CORE
M8	-	GND
M9	-	GND
M10	-	GND
M11	-	GND
M12	-	GND
M13	-	GND
M14	-	GND
M15	-	GND
M17	-	3.3V_IO
M18	-	GND
M19	I/OPD	**GPIO_19** / UTP_RX_DATA_7
M20	I/OPD	**GPIO_18** / UTP_RX_DATA_6
M21	I/OPD	**GPIO_17** / UTP_RX_DATA_5
M22	I/OPD	**GPIO_16** / UTP_RX_DATA_4
N1	O	DDR_SCLK_N
N2	O	DDR_DQM_0
N3	O	DDR_DQM_1
N4	I/O	DDR_DQS_0
N5	-	GND
N6	-	1.8V_CORE

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
N8	-	GND
N9	-	GND
N10	-	GND
N11	-	GND
N12	-	GND
N13	-	GND
N14	-	GND
N15	-	GND
N17	-	3.3V_IO
N18	-	GND
N19	I/OPD	**GPIO_12** / UTP_RX_DATA_0
N20	I/OPD	**GPIO_13** / UTP_RX_DATA_1
N21	I/OPD	**GPIO_14** / UTP_RX_DATA_2
N22	I/OPD	**GPIO_15** / UTP_RX_DATA_3
P1	O	DDR_SCLK
P2	-	GND
P3	O	DDR_CLKE
P4	O	DDR_ADDR_12
P5	O	DDR_ADDR_11
P6	-	1.8V_CORE
P8	-	GND
P9	-	GND
P10	-	GND
P11	-	GND
P12	-	GND
P13	-	GND
P14	-	GND
P15	-	GND
P17	-	1.8V_CORE
P18	O	UTP_RX_ADDR_2
P19	O	UTP_RX_ADDR_1

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
P20	O	UTP_RX_ADDR_0
P21	O	UTP_RX_EN_N
P22	I	UTP_RX_CLAV
R1	O	DDR_ADDR_5
R2	O	DDR_ADDR_6
R3	O	DDR_ADDR_7
R4	O	DDR_ADDR_8
R5	O	DDR_ADDR_9
R6	-	2.5V_IO
R8	-	GND
R9	-	GND
R10	-	GND
R11	-	GND
R12	-	GND
R13	-	GND
R14	-	GND
R15	-	GND
R17	-	1.8V_CORE
R18	I/OPD	AFE_DAC_6
R19	I/OPD	AFE_DAC_7
R20	O	UTP_TX_PRTY
R21	I	UTP_RX_PRTY
R22	I	UTP_RX_SOC
T1	O	DDR_ADDR_4
T2	O	DDR_ADDR_3
T3	O	DDR_ADDR_2
T4	O	DDR_ADDR_1
T5	O	DDR_ADDR_0
T6	-	2.5V_IO
T17	-	3.3V_IO
T18	I/OPU	AFE_DAC_5
T19	I/OPD	AFE_DAC_4
T20	I/OPD	AFE_DAC_3
T21	I/OPD	AFE_DAC_2

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
T22	I/OPD	AFE_DAC_1
U1	O	DDR_CS_0_N
U2	O	DDR_CS_1_N
U3	O	DDR_BA_0
U4	O	DDR_BA_1
U5	O	DDR_ADDR_10
U6	-	2.5V_IO
U7	-	3.3V_IO
U8	-	1.8V_CORE
U9	-	1.8V_CORE
U10	-	1.8V_CORE
U11	-	3.3V_IO
U12	-	3.3V_IO
U13	-	3.3V_IO
U14	-	1.8V_CORE
U15	-	1.8V_CORE
U16	-	3.3V_IO
U17	-	3.3V_IO
U18	I/OPD	AFE_ADC_2
U19	I/OPD	AFE_ADC_3
U20	I/OPD	AFE_SYNCOUT
U21	I/O	AFE_MCLK
U22	I/OPD	AFE_DAC_0
V1	-	SSTL2_REFGEN_1.25V
V2	O	DDR_SRAS_N
V3	O	DDR_SCAS_N
V4	O	DDR_SWE_N
V5	I/O	DDR_DATA_7
V6	I/O	**PCI_AD_5** / DSP0_EINT_N
V7	I/O	**PCI_AD_6** / DSP0_ECLK
V8	I/O	**PCI_AD_14** / DSP1_EINT_N
V9	I/O	**PCI_AD_15** /

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
		DSP1_ECLK
V10	-	GND
V11	-	GND
V12	-	GND
V13	-	GND
V14	I/O	**PCI_AD_26** / EJTAG_PCST_6
V15	I/O	**PCI_AD_27** / EJTAG_PCST_7
V16	O	PCI_EXT_2_GNT_N
V17	O	PCI_EXT_1_GNT_N
V18	I/OPD	SPI_SDATA
V19	I/OPD	AFE_ADC_1
V20	I/OPD	AFE_ADC_0
V21	I/OPD	AFE_SDIN
V22	I/OPD	AFE_SEN
W1	I/O	DDR_DATA_2
W2	I/O	DDR_DATA_3
W3	I/O	DDR_DATA_4
W4	I/O	DDR_DATA_5
W5	I/O	DDR_DATA_6
W6	I/O	**PCI_AD_4** / DSP0_EMS_N
W7	I/O	**PCI_AD_7** / DSP0_ELIN
W8	I/O	**PCI_AD_13** / DSP1_EMS_N
W9	I/O	PCI_CBE_1
W10	I/O	PCI_TRDY_N
W11	I/O	PCI_CLKRUN_N
W12	I/O	**PCI_AD_19** / EJTAG_TPC_2
W13	I/O	**PCI_AD_20** / EJTAG_PCST_0
W14	I/O	**PCI_AD_25** / ETJAG_PCST_5
W15	I/O	**PCI_AD_28** /

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
		EJTAG_PCST_8
W16	I	PCI_EXT_2_REQ_N
W17	I	**PCI_GNT_N** / PCI_EXT_3_REQ_N
W18	I/OPD	SPI_MDATA
W19	I/OPU	**GPIO_0** / SPI_ERROR / SPI_CS
W20	I	DSP0_SPORT0_DR / DSP1_SPORT0_DR
W21	O	AFE_SCLK
W22	O	AFE_SDOUT
Y1	I/O	DDR_DATA_1
Y2	I/O	DDR_DATA_0
Y3	I/OPD	**GPIO_25** / SPORT2_RSCLK
Y4	I/OPD	**GPIO_24** / SPORT2_TSCLK
Y5	I/OPD	**GPIO_26** / SPORT2_TFS
Y6	I/O	**PCI_AD_3** / DSP0_ERESET_N
Y7	I/O	PCI_CBE_0
Y8	I/O	**PCI_AD_12** / DSP1_ERESET_N
Y9	I/O	PCI_PAR
Y10	I/O	PCI_DEVSEL_N
Y11	I/O	**PCI_IRDY_N** / EJTAG_DCLK
Y12	I/O	**PCI_AD_18** / EJTAG_TPC_1
Y13	I/O	**PCI_AD_21** / EJTAG_PCST_1
Y14	I/O	**PCI_AD_24** / ETJAG_PCST_4
Y15	I/O	**PCI_AD_29** / EJTAG_PCST_9
Y16	I	PCI_EXT_1_REQ_N
Y17	I/O	PCI_INTA_N

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
Y18	I/OPD	SPI_CLK
Y19	I/OPU	**GPIO_1** / SPI_CS1_OUT
Y20	I/OPD	**GPIO_11** / DSP1_PF3
Y21	I/O	DSP0_SPORT0_RFS / DSP1_SPORT0_RFS
Y22	O	DSP0_SPORT0_DT / DSP1_SPORT0_DT
AA1	I/O	DSP0_SPORT1_TFS / DSP1_SPORT1_TFS
AA2	I/O	DSP0_SPORT1_SCLK / DSP1_SPORT1_SCLK
AA3	IPD	SPORT2_DR
AA4	I/OPD	**GPIO_27** / SPORT2_RFS
AA5	O	SPORT2_DT
AA6	I/O	**PCI_AD_2** / DSP0_EBG_N
AA7	I/O	**PCI_AD_8** / DSP0_ELOUT
AA8	I/O	**PCI_AD_11** / DSP1_EBG_N
AA9	I/O	PCI_SERR_N
AA10	I/O	PCI_STOP_N
AA11	I/O	PCI_FRAME_N
AA12	I/O	**PCI_AD_17** / DSP1_ELOUT
AA13	I/O	**PCI_AD_22** / EJTAG_PCST_2
AA14	I/O	PCI_CBE_3
AA15	I/O	PCI_PME_N
AA16	O	**PCI_REQ_N** / PCI_EXT_3_GNT_N
AA17	I	PCI_CLK_I
AA18	O	PCI_CLK_O
AA19	I/OPD	**GPIO_2** / SPI_CS2_OUT
AA20	I/OPD	**GPIO_10** / DSP1_PF2
AA21	I/OPD	GPIO_7

PIN	Pad Type	SIGNAL [In case of Muxed pins, the first function (in bold) is the "default"]
AA22	I/O	DSP0_SPORT0_TFS / DSP1_SPORT0_TFS
AB1	-	GND
AB2	O	DSP0_SPORT1_DT / DSP1_SPORT1_DT
AB3	I/O	DSP0_SPORT1_RFS / DSP1_SPORT1_RFS
AB4	I	DSP0_SPORT1_DR / DSP1_SPORT1_DR
AB5	I/O	**PCI_AD_0** / DSP0_EE
AB6	I/O	**PCI_AD_1** / DSP0_EBR_N
AB7	I/O	**PCI_AD_9** / DSP1_EE
AB8	I/O	**PCI_AD_10** / DSP1_EBR_N
AB9	I/O	PCI_PERR_N
AB10	I	PCI_LOCK_N
AB11	I/O	PCI_CBE_2
AB12	I/O	**PCI_AD_16** / DSP1_ELIN
AB13	I/O	**PCI_AD_23** / EJTAG_PCST_3
AB14	I	PCI_IDSEL_N
AB15	I/O	**PCI_AD_30** / EJTAG_PCST_10
AB16	I/O	**PCI_AD_31** / EJTAG_PCST_11
AB17	I/O	PCI_RST_N
AB18	-	NC
AB19	I/OPD	**GPIO_8** / DSP0_PF2
AB20	I/OPD	**GPIO_9** / DSP0_PF3
AB21	I/O	DSP0_SPORT0_SCLK / DSP1_SPORT0_SCLK
AB22	-	GND

4 Feature Summary

4.1 Hardware Features

4.1.1 ADSL/ADSL2/ADSL2+ CPE (ATU-R) DIGITAL DATA PUMP

4.1.1.1 ADSL

- Compliant with ITU G.992.1 and G.992.2 (Annexes A, B, and C Modes of Operation); ANSI T1.413 Issue 2; and ETSI ETR328 ADSL Standards
- G.dmt S=1/2 High Data Rate Downstream Mode
- Supports Trellis-Coded Modulation, Analog and Digital Echo Cancellation and Dual Latency with Programmable Priority
- Supports DSL Forum TR-048, Deutsche Telekom UR-2 and Other Published Testing/Qualification Standards

4.1.1.2 ADSL2/ADSL2plus

- Compliant with ITU G.992.3, G.992.4, G.992.5 ADSL2 and ADSL2plus (Annexes A, B, C, I, J, L, and M Modes of Operation)
- Supports data rates of up to 28 Mbps downstream and 3 Mbps upstream
- Support for INP values of S = 1/16 and D = 511
- Supports Two Bearer Channels and Two Latency Paths
- Supports Hardware for Decoupling of PMD and PMS Layers
- Supports Arbitrary Rational Multi-frame Code Word Parameter Sp Down to 1/3
- Supports 256 or 512 Tones in the Downstream
- Supports 1-Bit Constellations with Trellis-Coded Modulation
- Supports Reduced-Overhead Framing
- Supports Non-Integer Number-of-Bytes-per-DMT Symbol
- Supports All Specified Low-Power Modes (L0, L2, and L3)
- Supports All Required and Optional Online
- Reconfiguration (OLR) Modes including Seamless Rate Adaptation

4.1.2 Networking Micro-Architecture (based on Fusiv™)

- 32-bit, 200 MHz RISC processor (CPE – Control Processing Engine) - (16KB instruction cache, 8KB data cache)
- 2 DSPs, each running at 100MHz (72KB PM and 48KB DM in each DSP)
- One 200 MHz Accelerator Processor for ATM (8KB program memory, 4KB data memory)
- One 200 MHz Accelerator Processor for Buffer Management (8KB program memory, 2KB data memory)
- One 200 MHz Peripheral Accelerator Processor (8KB program memory, 2KB data memory)
- Two 200 MHz Accelerator Processors for Ethernets (8KB program memory, 2KB data memory in each Accelerator)
- Seven channel independent DMA to perform memory-to-memory and memory-to-peripheral data transfers.
- Boot through SPI EEPROM.
- Interfaces such as PCI, UTOPIA, USB 2.0 FS device and USB2.0 HS/FS/LS Host, UARTs and General Purpose Timers
- Specialized SPORT interface for universal connectivity.

4.1.2.1 Physical Interfaces

- On-chip DDR Controller for 16-bit DDR
- On-chip Asynchronous Memory Controller for Asynchronous RAM and FLASH
- Supports TWO 10 x 100 Ethernet Interfaces
- Data (DAC/ADC) and Control (SPORT-type) Interfaces for ADSL2/ADSL2plus AFE and Line Driver
- 33 MHz, 32-bit, PCI 2.2 Interface, which can work both in “host” and “device” modes.
- USB 2.0 FS device only
- USB 2.0 HS/FS/LS Host
- UTOPIA L1/L2 interface for ATM bonding option.
- Serial Interfaces
  - Asynchronous Serial Port (UART) 1 & 2
  - Serial Peripheral Interface (SPI)
  - Two SPORT Interfaces for DSP subsystem
  - Additional SPORT Interface on System Bus (DBUS2)
- General Purpose IO (GPIO)
- IEEE 1149.1 compliant JTAG

4.1.2.2 Electrical Characteristics

- 3.3V and 2.5V I/O and 1.8V core power supply. 2.3W (1.85W core power, 0.45W I/O power)

5 Hardware Description

Fusiv® Vx 160 is a system on chip integrating a Control Processing Engine (CPE), DSP subsystem for voice processing, and the following peripheral interfaces: two Ethernet 10/100 MIIs, USB 2.0 FS device, USB 2.0 HS/FS/LS host, PCI, UTOPIA, AFE, AFE DAC & ADC, SPI, two UARTs, three SPORTs, General Purpose I/O, DDR controller for interfacing 16-bit DDR-SDRAM and AMC (Asynchronous memory controller) for interfacing FLASH and Asynchronous SRAM.

The processing capabilities of Fusiv® Vx 160 device are augmented by the presence of multiple micro-coded Accelerator Processors. These APs are strategically located in the data paths of communication peripherals, to enable wire-speed performance. This leads to the advantage of the CPE having additional processing time for more powerful control and management functions.

A detailed description of the hardware architecture is given in Figure 1. Features of the various modules of Fusiv® Vx 160 are described below:

5.1 Control Processing Engine (CPE)

- 32-bit RISC engine
- Frequency: 200 MHz
- 16K Instruction Cache and 8K Data Cache
- EJTAG Support for debugging
- Optional 64 TLB Entry MMU
- 32-bit MAC

5.2 DSP Subsystem

- 2 DSPs with 100 MIPS each.
- 72KB of Program Memory in each DSP
- 48KB of Data Memory in each DSP
- EZ-ICE support for Emulator Control. EZ-ICE pins are multiplexed with PCI pins.
- Two SPORT interfaces to connect to hardware CODEC chips.

- The Host Interface is through IDMA interface built inside.
- Processing Power for 2 to 8 Voice Channels.

5.3 AFE (ADSL2/ADSL2plus) Interface

- AFE Interface for ADSL2/ADSL2plus AFE and Line Driver
- Dedicated serial port interface for AFE control and data, with 8-bit DAC and 4-bit ADC
- Physical bus interfaces for the AFE data path.
- Supports data rates of up to 28 Mbps downstream and 3 Mbps upstream.

5.4 Asynchronous Memory Controller (AMC)

- Supports Asynchronous/FLASH memory up to 64 MB/16MB respectively
- Supports asynchronous interface with programmable wait states

5.5 DDR Controller

- Frequency: 200 MHz
- Supports different configurations of 16-bit DDR up to 256 MB
- Supports Industry standard Double Data Rate (DDR SDRAM) from 64 Mbit to 512 Mbit device sizes with configuration of x4, x8, x16
- Supports up to 2 External Banks
- Page Hit Detection to support multiple column accesses with in same row.
- 8 internal row address registers to keep track of 8 open rows (2 chip selects with 4 internal banks each).
- Supports Fixed DDR SDRAM Burst Length of 2 only
- Programmable DDR SDRAM access timing parameters
- Automatic Refresh generation with programmable refresh intervals
- Supports Self-Refresh mode to reduce system power consumption

5.6 Ethernet 10/100 Controller (EMAC)

- Two built-in controllers
- Performs IEEE-802.3 framing

- Access via MII Interface (Compliant with IEEE-802.3 MAC protocol)
- Supports PAUSE Operation
- Dedicated Accelerator Processor, (one for each EMAC), for per packet processing. Features are as below:
  - 8KB of Program Memory, 2KB of Data Memory
  - Performs IP Version, TTL, check sum checks
  - Identifies the flow (by computing hash)
  - Checks for protocol anomaly attack
  - Updates per flow packet counters used for flood attack and activity detection
  - Performs routing and/or bridging functions by modifying MAC, IP and port numbers appropriately
  - Performs TTL decrementing and check sum updates
  - Fetches the table entry from DDR-SDRAM
  - Classifies the packet
  - Fetches buffers from buffer manager
  - Performs DMA transfers to/from the DDR-SDRAM
  - Queues buffers on to the egress Ports
  - Processes buffers queued for transmission
  - Performs QOS-based traffic management functions
  - Frees the buffers after transmission
  - VLAN processing

5.7 Buffer Manager/Queue Manager (BM)

- Architected around a dedicated accelerator processor for flexibility and high performance
- 8KB of Program Memory, 2KB of Data Memory
- Performs buffer allocation and de-allocation
- Maintains multiple types of buffers
- Initialization of headers for the structures allocated
- Performs classification for frames received from ATM interface.
- Addition of EMAC header for sending data directly to the egress port

5.8 Peripheral Accelerator Processor (Per AP)

- Architected around a Peripheral Accelerator Processor or as a Custom Accelerator Engine for flexibility and high performance
- As a Peripheral Accelerator Processor for the PCI interface, the AP can help support wire-speed, PCI-based WLAN applications
- 8KB of Program Memory, 2KB of Data Memory

5.9 On Chip DMA Controller (DMA)

- Scatter/Gather DMA
- Memory-to-Memory and Memory-to-Peripheral transfers
- Performs on-the-fly AAL5 CRC calculation
- Interfaces with SPORT2 block for efficient data transfers
- 7 Channel DMA

5.10 UTOPIA Interface (ATM)

- UTOPIA L1/L2 support
- On-the-fly header insertion into the ATM packet for 64 VCCs
- Dynamic CRC calculation for 64 VCCs (AAL5) on transmit side
- Per VCC AAL5 CRC calculation and header matching in the Receive direction for up to 64 VCCs.
- Can connect a maximum of three external UTOPIA PHY devices and one integrated PHY
- Dedicated APU with 8KB of Program Memory, 4KB of Data Memory
- APU performs SAR and TM functions

5.11 USB 2.0 FS device

- USB2.0 FS compliant device type interface
- Provides a flexible programming environment with up to seven endpoints
- Each endpoint can support all of the USB data types: Control, Bulk, Interrupt, and Isochronous
- Dedicated 2KB of memory for data storage

5.12 USB 2.0 Host

- USB2.0 HS/FS/LS compliant Host
- 272 bytes of Buffer Descriptor Memory and 4KB of Data Memory
- Supports both EHCI and OHCI
- Integrates UTMI+ PHY.

5.13 PCI Interface

- PCI 2.2 compliant
- 32 bit, 33 MHz Interface
- Supports PCI Host mode (Central resource) operation and PCI Device mode operation programmable by a control bit. Supports 23devices in Host Mode.
- PCI Master Operations and Target Operations
- Support four memory windows to be opened up for external master access.
- Back-to-Back PCI Transaction support
- Support for INTA
- Supports error reporting for fatal and parity errors on PCI bus
- Supports PERR, SERR signals
- Supports power management interface, #PME signal generation
- Supports dynamic Endian conversion based on the data type (BD, SA, CSR or Data)
- PCI Controller can be switched to work as Card Bus Controller, i.e., it provides Card Bus support. (The Card Bus is an extension to the PCI Bus.)

5.14 Arbiters

- Separate arbiter for each Bus
- Masters are grouped into two groups - processor and peripherals
- Priority-based arbitration across groups
- Round Robin arbitration within a group
- Bus Parking

5.15 SPORT on System Bus (SPORT2)

- SPORT interface on System Bus (DBUS2).
- Supports 3 to 32 bit serial data length.
- Dedicated central DMA channels for Tx & Rx data flows.

5.16 Asynchronous Serial Port (UART)

- Two UARTs, one dedicated and the other multiplexed with GPIOs
- Multiplexed UART supports flow control modes with RTS/CTS pins
- RTS and CTS are also multiplexed with GPIOs
- Data Length: 7,8 bits
- Parity: Even/Odd
- Baud Rate: 2400, 4800, 9600, 19200, 38400, 57600, 115200, 921600, 6250000 bps
- For debugging and also to connect to console and other devices

5.17 Serial Peripheral Interface (SPI)

- Baud Rate: Programmable up to 25 Mbps
- Data Exchange Mode: Interrupt
- Supports SPI master and Slave modes
- SPI master can address two SPI slaves.
- Data Length: 8, 16 bits
- FUSIV® VX 160 to be connected to Serial PROM with 16-bit address for SPI-based boot.

5.18 On-chip memory (LMEM)

- Single ported SRAM of size 2 KB.
- Read/Write access done in word, half word, byte modes
- Zero latency for write cycles
- Single clock latency for read cycles

5.19 Timers

- Three 32-bit Timers for CPE
- One Watch Dog Timer
- Optional interrupt generation near expiry time
- One 16-bit Timer per APU for traffic management.

5.20 General Purpose I/O (GPIO)

- 32 bit-wise programmable pins are provided as general purpose I/O (some pins are multiplexed with peripheral interfaces, can be freed as GPIO when the interfaces are not in use).
- These signals can be used to control LEDs and switches.

5.21 Clock Unit

- Five on-chip PLLs (PLL1, PLL2, PLL3, PLL4 and PLL5) with programmable VCO (Voltage Control Oscillator) frequency.
- PLL1 generates USB clock (48MHz).
- PLL2 generates System clock (100MHz), CPE clock (200MHz) and APU clock (200MHz).
- PLL3 generates ADSL2 high-speed clock (175MHz), low speed clock (87.5MHz) and AFE clock (35.328MHz).
- PLL4 generates PCI clock (33.33 MHz)
- PLL5 generates DSP subsystem clock (200MHz – DSP clock is in multiples of 2.048 / 4.096 MHz).

5.22 Interrupt Controller

- Supports up to 11 prioritized internal interrupts driven from the devices to the CPE
- Routes interrupts from all peripherals to PCI and Accelerator Processors

5.23 Reset Module

- Boot Up via SPI or FLASH is controlled by MII1_TX_DATA_0 pin during Power on Reset (POR)
- The chip is kept in reset for 50 cycles after POR is de-asserted

5.24 Power Management of all the blocks

- Gated clocks for all the modules
- Clocks for blocks in use should be switched on during boot-up

5.25 Test and Debug Block (TAD)

- IEEE 1149.1 compliant JTAG TAP controller for boundary scan
- JTAG support provides access to the CPE TAP controller for EJTAG support, which facilitates debugging of embedded software code.
- The CPE EJTAG 1.5.3 compliant controller has the following features:
  - External access to Fusiv® Vx 160 resources
  - Setting hardware breakpoints on internal cache buses
  - Single-step execution mode
  - Real-time program-counter trace

5.26 Buses

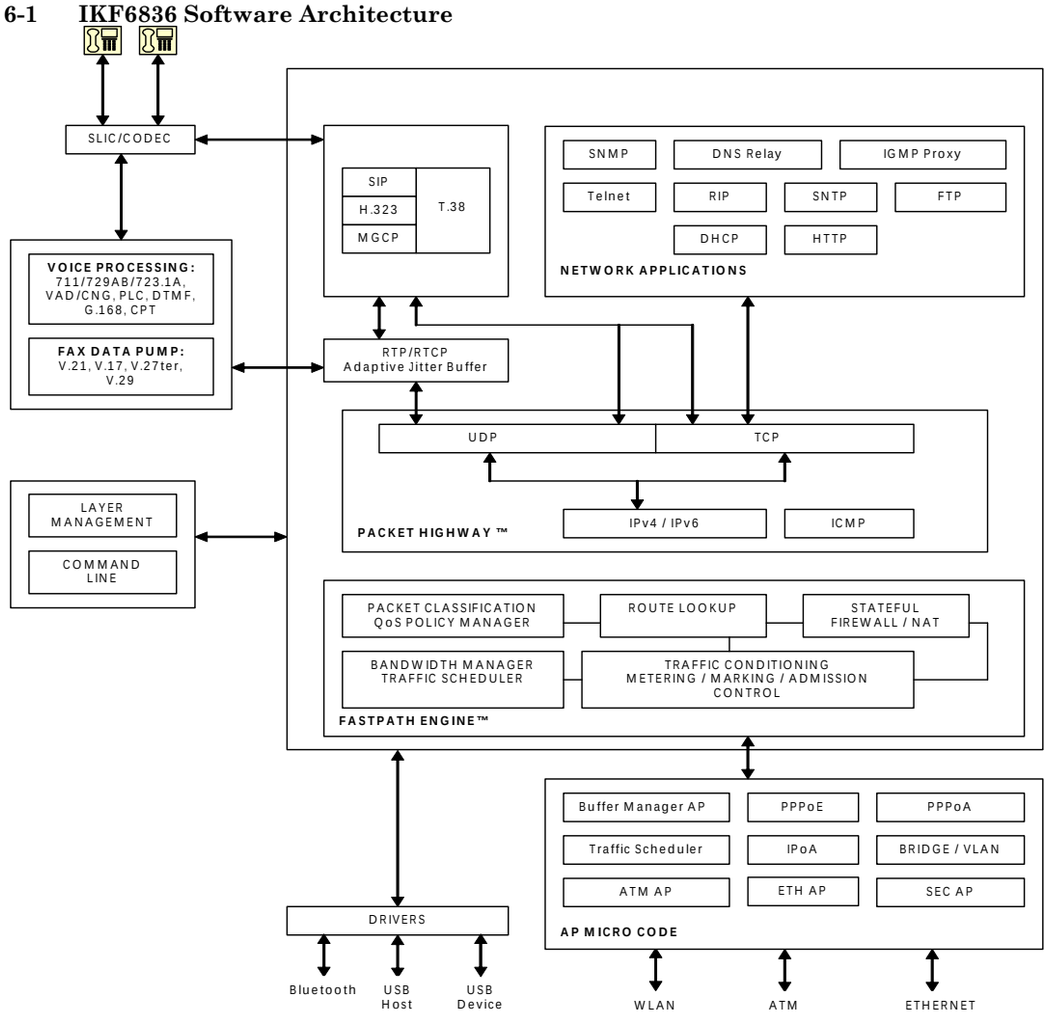
- System Bus (SBUS).
  - Three high performance backbone buses form the chip's System Bus.
  - Each of the buses is full-fledged with address, data and control lines of its own.
  - According to their significant functions, they are names Data Bus 1 (DBUS 1), Data Bus 2 (DBUS 2) and Control Bus (CBUS).
  - All the buses operate under multi-master environments and each has an Arbiter to allot buses to various masters in the chip.
  - Bridge BR 1 from DBUS 1 to DBUS 2 converts "bus transfers" into suitable format for slave devices on DBUS 2.
  - The Bridge provides latching of all addresses, data and control signals, and generates Slave select signals to peripherals on DBUS 2.
- Peripheral Bus (PBUS)
  - Low speed peripherals such as UART and GPT reside on this bus.
  - The peripheral bus is connected to CBUS by bridge BR 2.
  - The peripherals on PBUS are Slaves on the bridge BR 2.
  - Bridge BR 2 provides latching of all addresses, data and control signals, and generates Slave select signals to the peripherals on the PBUS.

6 Software Description

Fusiv® Vx 160 is integrated with two basic software bundles: Data-centric Routing with Voice over IP. The Fusiv® Vx 160 software bundle comes with needed processing and signaling modules for VoIP. Fusiv® Vx 160 is integrated with exhaustive software protocols and data-forwarding modules that are effectively integrated with hardware engines.

A Linux Board Support Package, Toolkit Driver and Reference Platform are provided with this solution. The software organization is shown in Figure below.

Figure 6-1 IKF6836 Software Architecture



6.1 Software Drivers

- The Drivers consist of the following:
- Linux Board Support Package
- Ethernet
- 802.11a/b/g
- USB Device and Host
- ATM
- ADSL Management Entity
- Accelerator Processor firmware and Host API
- Voice Framework

6.2 ATM WAN Processing

- ATM WAN processing software comprises:
- AAL5 (Hardware assisted SAR) (I.363.5)
- UNI 3.1
- ATM TM 4.0
- CBR, UBR, nrt-VBR, rt-VBR Support
- IPoA (RFC 2225)
- PPPoA (RFC 2364)
- Ethernet Bridging (RFC 2684)
- OAM F4/F5 (I-610)
- G.bond ADSL bonding

6.3 Network Software

- The Network Software consists of TCP/IP & related applications, Routing Protocols and Network Management Software:
- TCP
- UDP

- ICMP
- IPV4
- VLAN (802.1q)
- Bridge (802.1d)
- PPP
- PPPoE (RFC 2516)
- RIP V1, V2 (RFC 1058, RFC 2453)
- ARP
- RARP
- IGMP
- IGMP Proxy

6.4 BOOTP

- DHCP Client (RFC 2131)
- DHCP Server (RFC 2131)
- FTP
- TFTP
- DNS Relay
- SNTP (RFC 2030)
- SNMP V1, V2
- TELNET Server (for configuration)
- Command Line Interface
- Web Management
- Enterprise MIB

6.5 IP Services and QOS Software

- This consists of QoS / Bandwidth Management and Firewall Applications:
- DiffServ IP QoS Classification
- Traffic Conditioning

- WFQ-based Bandwidth Management
- NAT/Firewall - Packet Filtering
- PAT
- Stateful Firewall, Policy-based Filters

6.6 VoIP Voice Processing Software

- The VoIP Voice Processing software has the following features :
- Voice Compression – G.711 (PCMU & PCMA), G.729 A/B, G.723.1A
- G.168 Echo Canceller (Tail Length 32 ms)
- Voice Activity Detection (VAD)
- Comfort Noise Generation (CNG)
- Packet Loss Concealment (PLC)
- DTMF Detection and Generation
- DTMF Relay (RFC 2833)
- Call Progress Tone Generation
- FSK caller ID generation
- Country-specific standard tones support
- FAX pass through in addition to T.38 Fax relay
- The CPE supports the following fax data pump features:
- V.21 at 300bps binary signaling modem
- V.27ter @2.4Kbps or 4.8Kbps high speed modem
- V.29 @7.2Kbps/9.6Kbps high speed modem
- V.17 @7.2Kbps/9.6Kbps/12.0Kbps/14.4Kbps high speed modem
- CED & CNG Detection and Generation
- The CPE supports the following voice protocols with standard peripherals:
- RTP/RTCP
- Adaptive Jitter Buffer
- UDP support
- T.38 Real Time Fax Relay

- SIP (RFC 3261 and compatible with RFC 2543)
- ITU – T H.323 signaling and H.450 call features
- MGCP (RFC 3435 and compatible with RFC 2705)

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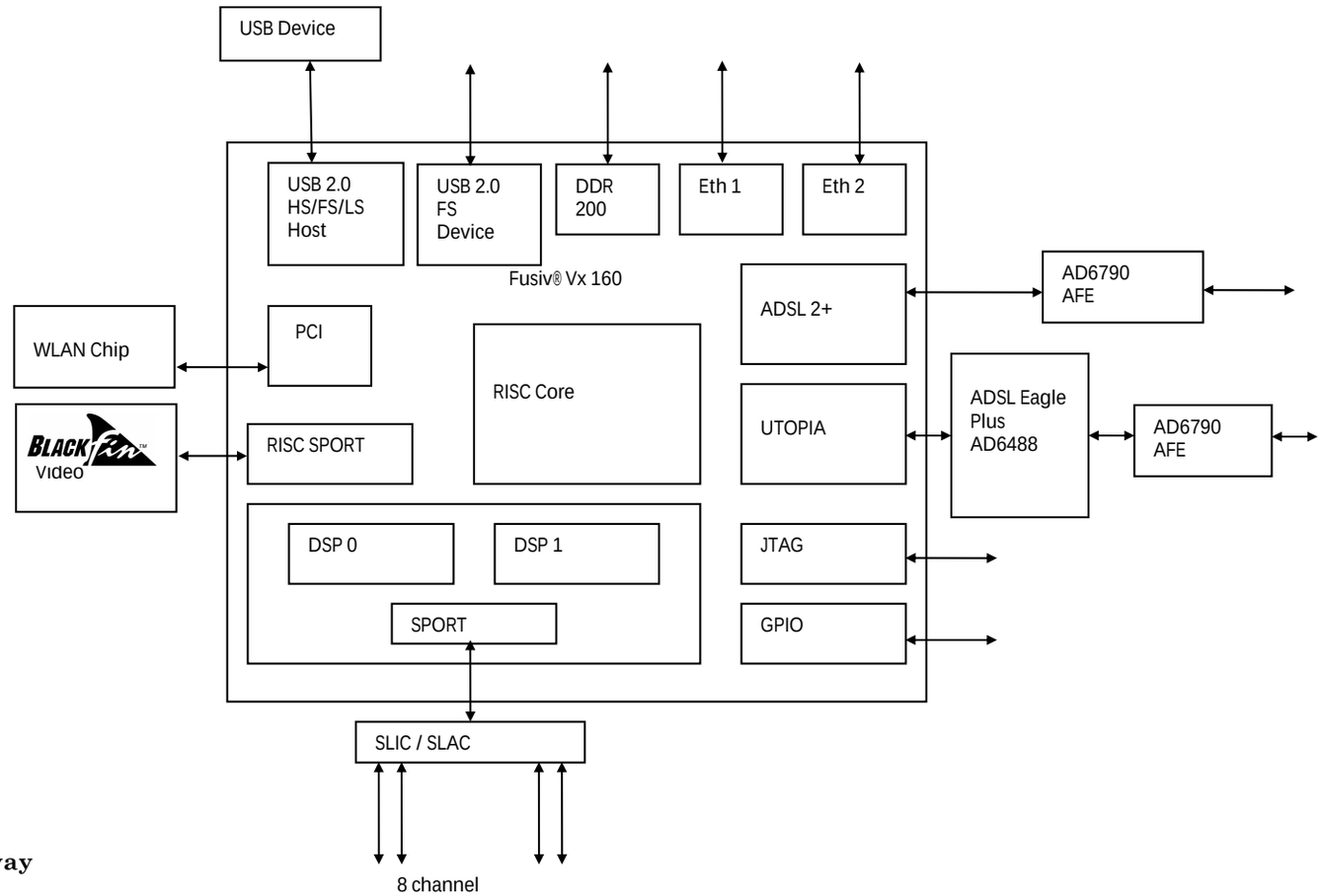
7 Applications

Fusiv® Vx 160 handles a range of voice solutions with its computation resources and multiple interfaces. The main applications are :

- VoIP Gateway
- ADSL Router with Bonding option
- Triple Play Gateway

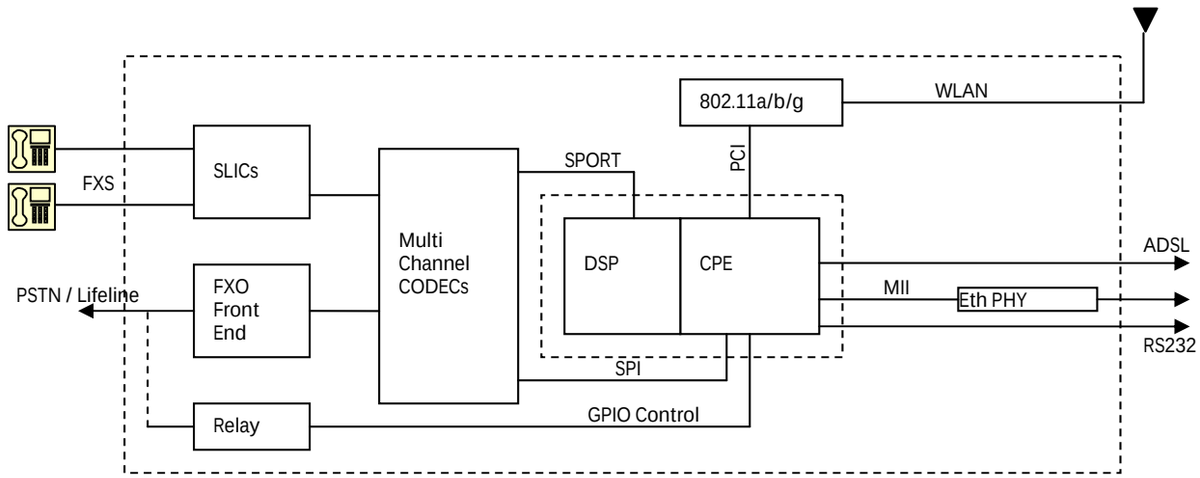
Figure 7-1 IKF6836 Applications



VoIP Gateway

A VoIP Gateway is a high-end VoIP adapter with numerous voice and data features, as shown in the figure below. An ADSL Data Pump is integrated.

Figure 7-2 VoIP Gateway



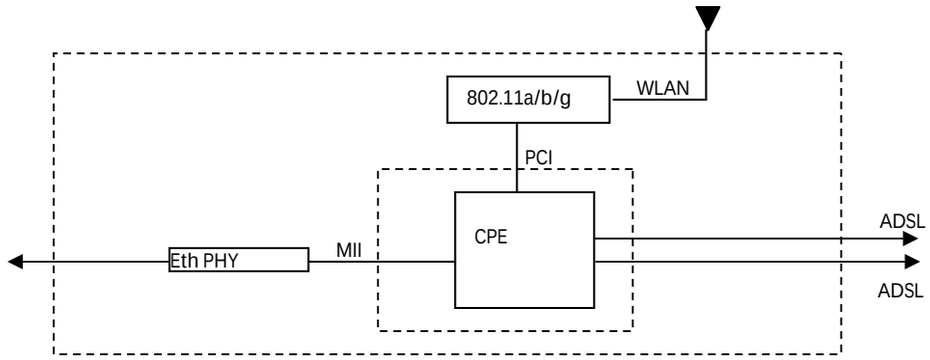
Voice entering through the telephone lines is collected through SLIC and CODEC interfaces. The CODEC (hardware device) samples the voice at a rate of 8 KHz. Voice samples are compressed in DSP and formed into compressed raw packets. The compressed packets go through the host processor. The host processor adds all the required headers and routes it to the right destination. Call establishing is mainly handled as signaling packets in the host processor. SLICs and CODECs report OFF-Hook, ON-Hook type of signaling status to the host RISC engine.

The host RISC Engine delivers Voice and Signaling packets on the Ethernet interface. The Ethernet interface joins with the service provider's network through a local modem, resident at the customer premises. Modems have Ethernet on the one side and DSL or Cable connectivity on the other side

ADSL Router with Bonded ADSL

An ADSL Router with Bonded ADSL allows greater data rate via extra ADSL connections.

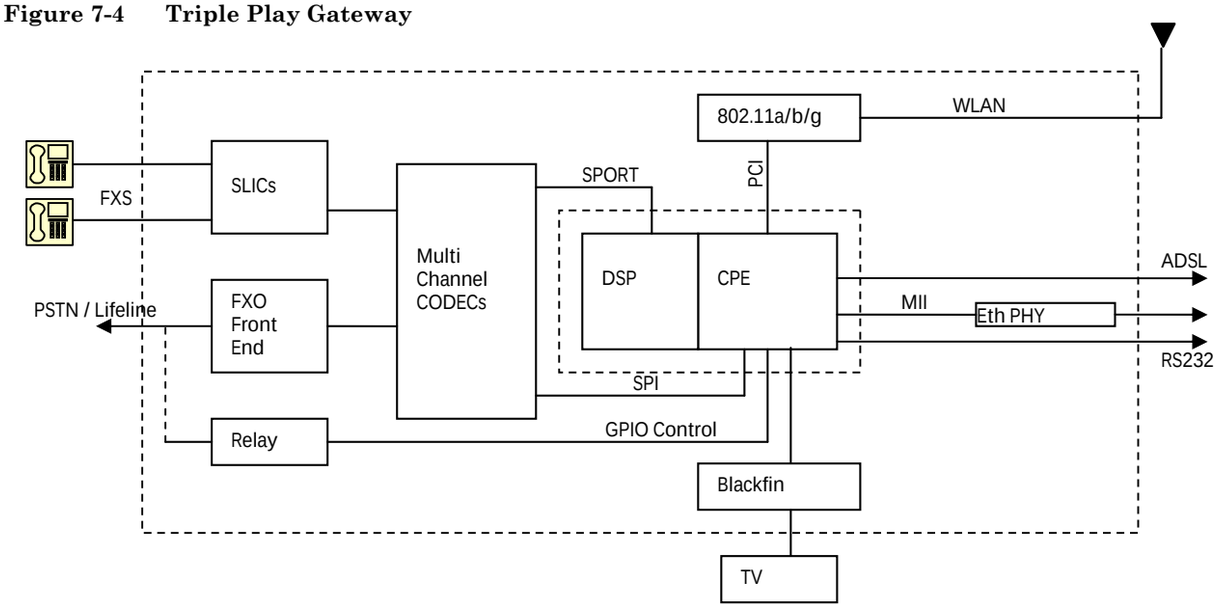
Figure 7-3 ADSL Router with Bonded ADSL



Triple Play Gateway

Adding Video decode with the ADI's Blackfin processor, triple play of Voice, Video and ADSL data routing is available as a well integrated solution

Figure 7-4 Triple Play Gateway



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8 Glossary

Table 8-1 Glossary

Acronym	Description
AAL5	ATM Adaptation Layer 5
ATM	Asynchronous Transfer Mode
ACL	Access Control list
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AH	Authentication Header
ALG	Application Level Gateway
APU	Accelerator Processor Unit
ATM	Asynchronous Transfer Mode
BD	Buffer Descriptor
BM	Buffer Manager
CBC	Cipher Block Chaining
CFB	Cipher Feedback
CMOS	Complementary Metal-Oxide Semiconductor
CODEC	Coder (ADC) and Decoder (DAC) hardware
CPE	Control Processor Engine
CRC	Cyclic Redundancy Check
CSR	Control and Status Register
CTR	Counter
DAC	Digital to Analog Converter
DES	Data Encryption Standard
DMA	Direct Memory Access
DSL	Digital Subscriber Line
DSP	Digital Signal Processing
EAP	Ethernet Accelerator Processor
EBIU	External Bus Interface Unit
ECB	Electronic Code Book
EEPROM	Electrically Erasable Programmable Read-only Memory
EMAC	Ethernet Media Access Controller
ESP	Encapsulated Security Payload
FIPS	Federal Information Processing Standards
GPIO	General Purpose Input Output
GPT	General Purpose Timer
HMAC	Hash Message Authentication Code
IP	Internet Protocol
IV	Initial Vector
LFSR	Linear Feedback Shift Register
LMEM	Local Memory
MBAR	Memory Base Address Register
MD5	Message Digest 5
MII	Media Independent Interface
MIPS	Million Instructions Per Second
MMU	Memory Management Unit
OFB	Output Feedback
PBGA	Plastic Ball Grid Array
PBX	Private Branch Exchange
PCI	Peripheral Component Interconnect
PHY	Physical Interface
PLL	Phase Locked Loop
POTS	Plain Old Telephone Service
RISC	Reduced Instruction Set Computer
RNG	Random Number Generator
SA	Security Association

Acronym	Description
SAR	Segmentation And Re-assembly
SCU	System Control Unit
SDRAM	Synchronous Dynamic Random Access Memory
SHA	Secure Hash Algorithm
SLIC	Subscriber Line Interface Circuit
SPE	Security Processing Engine
SPI	Serial Peripheral Interface
SPORT	Serial Port
SRAM	Static Random Access Memory
TAD	Test and Debug
TAP	Unit Test Access Port
TDES TLB	Triple Data Encryption Standard Translation Look

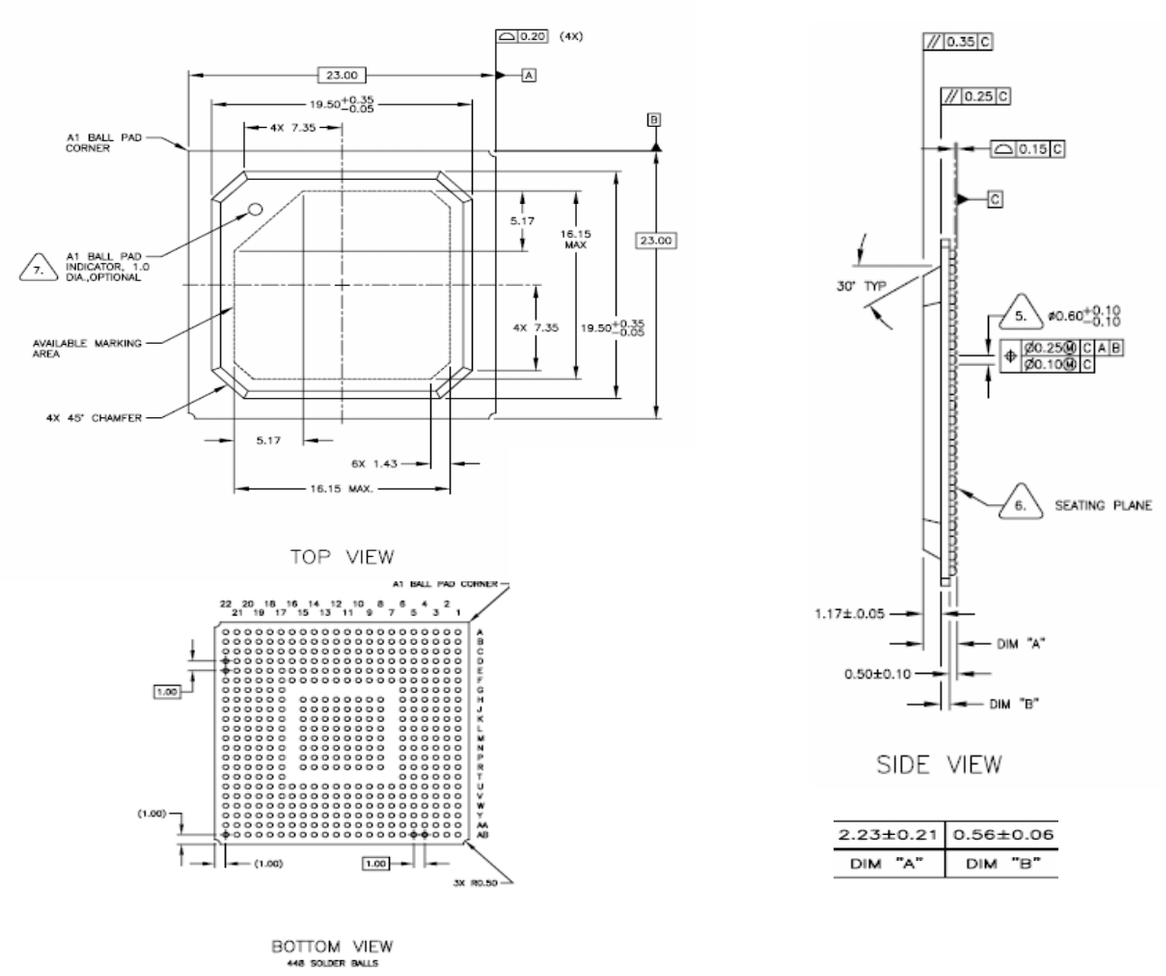
Acronym	Description
	aside Buffer
TM	Test Mode
TTL	Time To Live
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UTOPIA	Universal Test and Operation Physical Interface fo ATM
VCC	Supply Voltage
VCO	Voltage Control Oscillator
VLAN	Virtual Local Area Network
VoIP	Voice over IP

9 Mechanical Data

Figure 9-1 IKF6836 Package Outline Dimensions

448-PBGA (Lead free) 23 mm x 23 mm

Dimensions are shown in millimeters.



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10 Ordering Guide

Model	Temperature Range	Package Description	Package Option
IKF6836-A0-PB1-C	0^0 C to $+70^0$ C	Plastic Ball Grid Array	448 PBGA

10.1 Part Numbering Scheme

The following example explains the part numbering scheme

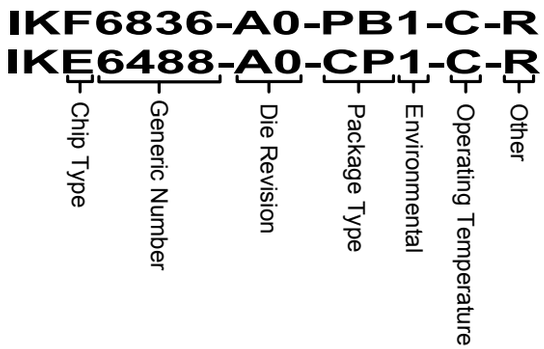


Table 10-1 Part Numbering Scheme

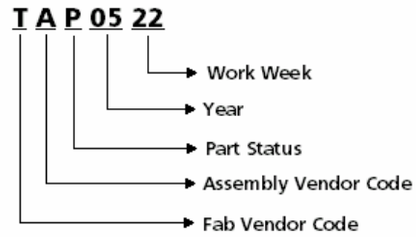
Chipset Type	Blank	Other
	D	Daughter Card (Ref Systems)
	E	Eagle
	F	Fusiv
Generic Number	XXXX	Chip Function
Package Type	BC	CSPBGA
	CP	LFCSP
	EB	EBGA
	HB	HSBGA
	LB	LBGA or MBGA

Table 10-2 Part numbering scheme (continued)

	PB	PBGA
	PF	FPBGA
	QE	Exposed TQFP
	QL	LQFP (1.4 mil)
	QM	MQFP (>1.4 mil)
	QT	TQFP (1.0 mil)
	TB	TBGA
	VB	VIPER
Environmental Parameter	0	Standard Package
	1	Lead Free (RoHS 5)
	2	Green (RoHS 6)
Operating Temperature	C	Commercial 0° to +70°C
	L	Industrial –40° to +85°C
Other	R	Tape and Reel
	Y	Special Customer Flow

10.2 Marking Data

Table 10-3 Marking Specification

Line #	Marking Specification	Example
1	IKANOS communications	IKANOS communications Eagle and / or Fusiv Logo
2	Part number	IKF6836-A0-
3	Package	PB1-C
4	Datacode	TAP0522:  See Table 10–4, Table 10–5, and Table 10–6 for legends on fab vendor code, assembly vendor code, and part status respectively.
5	Fab lot number	Fab lot number

10.3 Fab Vendor Code

Table 10-4 Fab Vendor Code

Foundry	Code Designator
TSMC	T
UMC	U
IBM	B
CHARTERED	C
TOWER	W
AMS	A
SAMSUNG	S
IMP	M

10.4 Assembly Vendor Code

Table 10-5 Assembly Vendor Code

Assembly Vendor	Code Designator
ASEK	A
SPIL	L
STATSChipPac-Singapore	S
OSE	O
STATSChipPac-China	H
STATSChipPac-Korea	R
UTAC	U
AMKOR-Philippines	P
AMKOR-Singapore	G
ASEM	M
ASECL	C

10.5 Part Status

Table 10-6 Part Status

Part Status	Code Designator
Production	P
Engineering	E
Marketing Sample	M